A CMOS ANALOG PULSE COMPRESSOR WITH A LOW-POWER ANALOG-TO-DIGITAL CONVERTER FOR MIMO RADAR APPLICATIONS

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A CMOS ANALOG PULSE COMPRESSOR WITH A LOW-POWER ANALOG-TO-DIGITAL CONVERTER FOR MIMO RADAR APPLICATIONS

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LIST OF SYMBOLS OR ABBREVIATIONS

ADC analog-to-digital converter.

AHN ad hoc network.

APC analog pulse compressor.

ASP analog signal processing.

AWG arbitrary waveform generator.

AWGN additive white Gaussian noise.

BW bandwidth.

CMOS complementary metal-oxide-semiconductor.

CP charge pump.

DAC digital-to-analog converter.

DC direct current.

DSP digital signal processor or digital signal processing.

ENOB effective number of bits.

FCP fast convolution processing.

FFT fast Fourier transform.

FIR finite impulse response.

FOM figure of merit.

FPGA field-programmable gate array.

IFFT inverse fast Fourier transform.

LPF low-pass filter.

LSB least significant bit.

MF matched filter.

MIMO multiple-input multiple-output.

MRSS multi-resolution spectrum sensing.

MSB most significant bit.

NLFM nonlinear frequency modulation.

NMOS n-type metal-oxide-semiconductor.

OFDM orthogonal frequency-division multiplexing.

PCB printed circuit board.

PM phase margin.

PMOS p-type metal-oxide-semiconductor.

PRF pulse repetition frequency.

PSRR power supply rejection ratio.

PVT process, supply voltage, and operating temperature.

RAM random-access memory.

RCS radar cross-section.

RF radio frequency.

RHP right half-plane.

SAR successive approximation register.

SAW surface acoustic wave.

SC switched capacitor.

S/H sample-and-hold.

SISO single-input single-output.

SNR signal-to-noise ratio.

SOC system-on-a-chip.

UWB ultra-wideband.

SUMMARY

Multiple-input multiple-output (MIMO) radars, which utilize multiple transmitters and receivers to send and receive independent waveforms, have been actively investigated as a next generation radar technology inspired by MIMO techniques in communication theory. Complementary metal-oxide-semiconductor (CMOS) technology offers an opportunity for dramatic cost and size reduction for a MIMO array. However, the resulting formidable signal processing burden has not been addressed properly and remains a challenge. On the other hand, from a block-level point of view, an analog-to-digital converter (ADC) is required for mixed-signal processing to convert analog signals to digital signals, but an ADC occupies a significant portion of a system's budget. Therefore, improvement of an ADC will greatly enhance various trade-offs. This research presents an alternative and viable approach for a MIMO array from a system architecture point of view, and also develops circuit level improvement techniques for an ADC.

This dissertation presents a fully-integrated analog pulse compressor (APC) based on an analog matched filter in a mixed signal domain as a key block for the waveform diversity MIMO radar. The performance gain of the proposed system is mathematically presented, and the proposed system is successfully implemented and demonstrated from the block level to the system level using various waveforms. Various figures of merit are proposed to aid system evaluations. This dissertation also presents a low-power ADC based on an asynchronous sample-and-hold multiplying SAR (ASHMSAR) with an enhanced input range dynamic comparator as a key element of a future system. Overall, with the new ADC, a high level of system performance without severe penalty on power consumption is expected.

The research in this dissertation provides low-cost and low-power MIMO solutions for a future system by addressing both system issues and circuit issues comprehensively.

CHAPTER I

INTRODUCTION

1.1 Motivation

Complementary metal-oxide-semiconductor (CMOS) technology offers an opportunity for dramatic cost and size reduction for a MIMO array. CMOS also offers mixed-signal integration opportunities for concurrent programmability. Therefore, there have been efforts to realize very-large-scale phased arrays ($\approx 10^6$ elements) based on CMOS such as in Figure 1. However, the increased burden on signal processing has not yet been discussed.

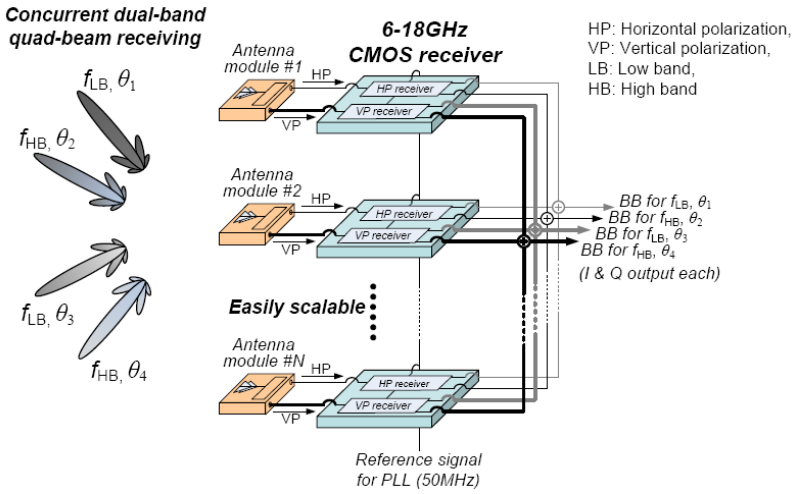


Figure 1: Scalable 6-to-18 GHz concurrent dual-band quad-beam phased array system [1].

Multiple-input multiple-output (MIMO) radars, which utilize multiple transmitters and receivers to send and receive independent waveforms, have been actively investigated as a next generation radar technology [2, 3]. Unlike previously well-known beamforming arrays, which have a high correlation between either transmitted or

received arrays of signals, the MIMO concept utilizes independence (i.e. low correlation) between signals. The beamforming array can steer a beam without mechanical elements by electrically phase shifting each array signal, but it is known that the beamforming array does not have processing gains [2]. The MIMO radar has been inspired by multiple-input multiple-output (MIMO) techniques in communication theory, which have already been incorporated into next generation communication standards [4] with orthogonal frequency-division multiplexing (OFDM). The MIMO technique utilizes many transmitting and receiving antennae as depicted in Figure 2.

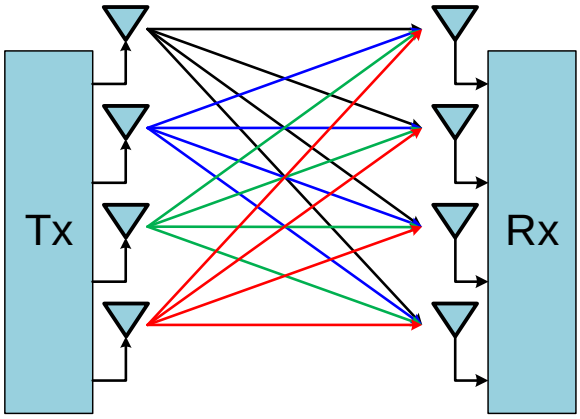


Figure 2: MIMO concept in communication system.

With MIMO radar, many independent radars collaborate to obtain diversity gain. Since a received signal is a superposition of independently faded signals, the average signal-to-noise ratio (SNR) is more or less constant, which is an important advantage over conventional radar. Therefore, MIMO radar is known to have more or less constant average SNR of the received signal unlike a conventional radar under Swerling models (See Figure 3).

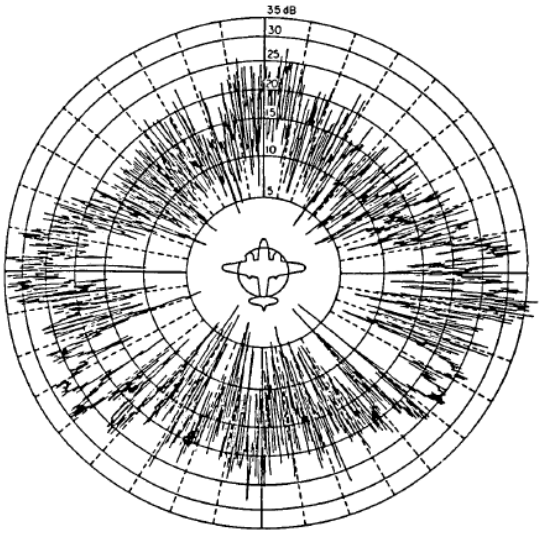


Figure 3: Measured radar cross-section (RCS) pattern of a B-26 bomber at 10-cm wavelength [5].

However, different transmit antennae need to see uncorrelated aspects of the target to achieve spatial diversity. Mathematically, this is expressed as orthogonality between signal vectors [2] as shown in Figure 4.

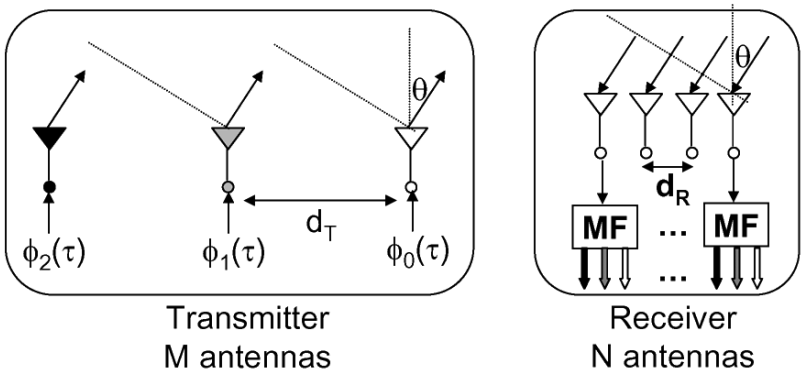


Figure 4: Illustration of a MIMO radar system [6].

The transmit antennae emit orthogonal waveforms $\phi_k(\tau)$, which are the extracted by matched filters (MFs) at each receiving antenna. Since MF is required for each receiver, a flexible (programmable), low-power MF is necessary to reduce total power consumption. In other words, the signal processing block has to generate the signals

for all transmitters and has to process the signals from all receivers, while at the same time all these signals are independent. Therefore, the signal processing burden and the power consumption of the analog-to-digital converter (ADC) increase rapidly with the number of array elements. This excessive demand on the signal processing power and the ADC can be a major hurdle to overcome for the MIMO radar. Furthermore, this significant burden can prevent combining the MIMO radar with different concepts such as an ad hoc network (AHN) [7] to implement a mobile-distributed MIMO radar.

One of the key building blocks in the MIMO radar system that this research focuses on is a pulse compressor, which is commonly implemented by a matched filter (MF). Radar range resolution, pulse width, and average transmitted power have a trade-off since the range resolution is $\Delta R = c\tau/2$ and the average transmitted power is $P_{av} = P_t \tau f_r$, where τ is radar pulse width, c is the speed of light, P_t is the peak transmitted power, and f_r is the pulse repetition frequency. In other words, for a better (or smaller) range resolution, the pulse width should be minimized, and the peak power of the radar increased to maintain the same average power. The pulse compressor allows high average transmitted power of a long pulse while maintaining high resolution of short pulses.

The lack of ADCs with sufficient speed and/or dynamic range constrains many radar designs [8]. Moreover, the speed requirements of an ADC keep increasing because of a modern direct-conversion architecture and high bandwidth waveforms, and the dynamic range requirement of an ADC keeps increasing to detect reduced signal returns in heavy clutter and electronic counter measure environments. The requirements for each ADC are increasing as well as the number of ADCs needed since one or two ADCs are required for each element either in beamforming arrays or in MIMO radars. Therefore, a low-power ADC is one of the key enabling technologies for MIMO radars in that it can enable MIMO radars to maintain the same total power consumption as that of single-input single-output (SISO) radars while keeping up with

the increased number and requirements of an ADC.

1.2 Organization of the Thesis

Based on the aforementioned technological background and motivation, the purposes of this work are as follows:

- To investigate architectures to construct an alternative pulse compressor architecture;
- To simulate the proposed architecture to verify the concept;
- To design and verify the functionality and performance of the APC in CMOS technology;
- To investigate a different architecture for a low-power ADC;
- To design the proposed ADC and an important sub-block such as a comparator at a circuit level.

Chapter 1 contains an introduction and the motivation for this work. To provide some background, Chapter 2 presents current challenges and existing technologies for an APC and an ADC. Also, a simple system-level mathematical framework is presented to justify the proposed approach. This chapter serves as a basis for the APC and the ADC presented in the following chapters. Chapter 3 presents a fully-integrated APC in the CMOS technology from the system level to a detailed circuit level. Measurement results and analyses of the results are presented in this chapter as well. Chapter 4 presents an enhanced input range dynamic comparator for an ADC, and Chapter 5 presents a new low-power ADC based on an asynchronous sample-and-hold multiplying successive approximation register (ASHMSAR). Finally, Chapter 6 summarizes and concludes the work in this dissertation by suggesting research directions for future research.

CHAPTER II

CHALLENGES AND TRENDS

2.1 Challenges

2.1.1 Pulse Compressor

As discussed earlier, MIMO radar application requires independent signals for the transmitters and receivers. The waveform flexibility is important because designing different integrated circuits for each individual waveform is not practical. Moreover, for future expansion to mobile applications, the architecture that is friendly to the system-on-a-chip (SOC) integration is desirable. Another very important aspect for these applications is low power consumption. In this sense, the design that can be implemented with CMOS technology will be desirable since the digital functionalities can be easily implemented by CMOS. Additionally, the cost for the unit transistor will decrease with aggressive gate length scaling.

2.1.2 Analog-to-Digital Converter (ADC)

Usually the final block of the signal processing chain in an analog or radio frequency (RF) communication system is an ADC. The processed signal is sampled by an ADC and then transferred into the digital domain for further processing, usually with a digital signal processor (DSP).

The commonly used figure of merit (FOM) for an ADC is [9]

$$\text{FOM}\,(\text{J/step}) = \frac{P}{2^{\text{ENOB}} \cdot f_s}, \tag{1}$$

where P is the power consumption, f_s is the sampling frequency, and ENOB is the effective number of bits. As this FOM suggests, the power has to be increased 3 dB for every bit increment or for every doubling of the sampling frequency. Even with

the improvement of the ADC in recent years [10], the ADC is still considered a high power consuming block, so it is not uncommon to determine the analog/RF front-end and ADC specifications based on the available power budget [11]. In other words, the specifications of available ADCs can have a great impact on the system architecture.

This trend applies to radar systems as well. As estimated in [12], the ADC power consumption occupies a significant portion of the total radar system power budget. Therefore, developing a low-power ADC that has a different architecture, which has the potential to break current trade-offs, could be beneficial for future MIMO radar systems.

2.2 Prior Arts

There are two well-known conventional approaches for the pulse compression. One is the surface acoustic wave (SAW) device-based [13] approach, and the other is the DSP-based approach, which is usually called fast convolution processing [14].

2.2.1 Surface Acoustic Wave (SAW) Device

SAW devices can be designed as filters matched to certain arbitrary waveforms, or they can be used as arbitrary waveform generators. Therefore, they have been widely used for pulse compression. A reflective SAW device is shown in Figure 5.

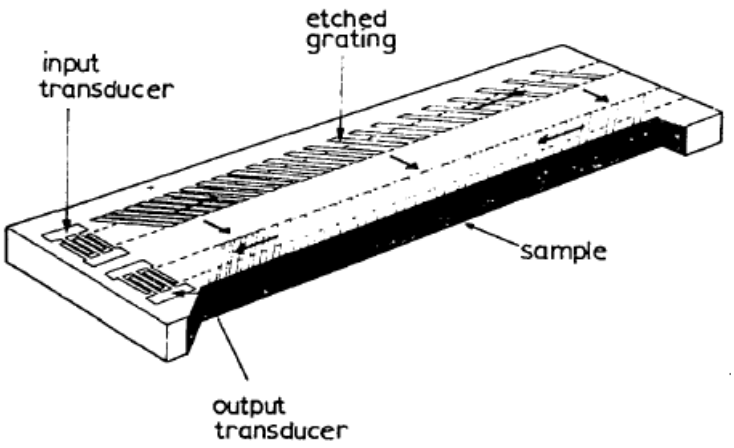


Figure 5: Diagram of an r.a.c. (reflective array compressor) device with internal weighting [13].

One drawback of using a SAW device is that piezoelectric materials such as quartz or lithium niobate are necessary to build high-quality SAW filters, so SOC integration is difficult. Also, SAW devices are not reconfigurable, so they are designed and used for only one pre-defined signal. Moreover, device size does not shrink as technology improves, unlike in CMOS technology, and devices are relatively expensive because of the custom fabrication requirement.

2.2.2 Digital Signal Processor (DSP)

DSPs have become more popular and powerful with their ever decreasing transistor size following the so-called Gene's law [15]. Therefore, performing matched filtering in the digital domain using DSPs is very attractive. Even though DSP computing power increases fast as process technology advances, matched filtering is still computationally expensive since this operation requires both the fast Fourier transform (FFT) and the inverse fast Fourier transform (IFFT). This computational burden could be especially significant for a MIMO system, with the computational burden translating into a power burden. Also, ADCs used for this architecture should have a high sampling rate and a wide dynamic range. The digital finite impulse response

(FIR) filter implementation of a MF [16] has similar problems.

2.2.3 Other Approaches

Various studies have been implemented to find alternatives to conventional approaches. Matched filters using capacitors as memory elements [17, 18] or using a charge-transferring mechanism [19] have been popular, but capacitor mismatches or charge leakages could be problematic, and it is difficult to implement a matched filter for long pulses. An approach based on a floating-gate MOS [20] could also have difficulties with long pulses, and an approach using a bank of digitally controlled transconductors along with capacitors [21] could suffer from transconductance mismatch. Other approaches such as the current-mode operation-based one [22] and the $\Sigma\Delta$ converter-based recycling integrator [23] could also suffer from mismatch problems or could have difficulties with long pulses.

2.2.4 Low-Power ADC

Even though many different types of ADCs exist, many of them require op amps to amplify the signals. In this case, large loop gain of the op amp will linearize the transfer function, and the ADC becomes robust to the disturbances such that power supply rejection, common mode rejection, process, supply voltage, and operating temperature (PVT) robustness will improve. However, it is known that the commonly used class-A op amp in a switched capacitor (SC) circuit is inherently inefficient [11]. Therefore, the ADCs that do not have op amps have been actively investigated in recent years. These include a comparator-based SC circuit [24, 25], an inverter-based $\Sigma\Delta$ modulator [26], and a comparator-based asynchronous successive approximation register (SAR) [27].

Another trend in recent years has been the so-called digitally assisted architecture. Due to the scaling of CMOS technology, digital circuits have become relatively inexpensive compared to analog circuits in SOC. Therefore, the digital-intensive ADC

architecture such as a $\Delta\Sigma$ modulator has become more attractive where the oversampling ratio of a $\Delta\Sigma$ modulator can be increased by the speed gain obtained through scaling. Other ADC architectures such as a pipeline ADC can benefit from this expansion of digital portion of an ADC as well. One of the approaches in this direction is digital calibration. Even though digital calibration has been well-known and widely used for high-resolution ADCs mostly [28], one very promising approach goes one step further to digitally correct errors caused by open-loop gain stages in the background so that high gain closed-loop op amps are no longer necessary [29].

2.3 Architecture Comparison

If different systems are to be compared, a figure of merit is necessary to quantify system performance in a concise way. However, selecting a good figure of merit is not an easy task since this figure of merit has to capture many different aspects of the system. In this section, a figure of merit based on the most commonly used figure of merit from ADC is proposed.

If an input signal to an ADC is a sine wave, then SNR is

$$\begin{aligned} \mathrm{SNR\,(dB)} &= 20\log_{10}\frac{V_{in,RMS}}{V_{Q,RMS}} \\ &= 20\log_{10}\frac{V_{REF}/(2\sqrt{2})}{V_{LSB}/\sqrt{12}} \\ &= 20\log_{10}\left(\sqrt{\frac{3}{2}}2^{\mathrm{ENOB}}\right) \\ &= 6.02\cdot\mathrm{ENOB}+1.76 \end{aligned} \tag{2}$$

which is a well-known formula. Since 2^{ENOB} is common for (1) and (2), 2^{ENOB} from (2) can be put into (1), and a modified Walden figure of merit for a system can be

defined as follows.

$$\begin{aligned} \text{FOM} &= \frac{P}{\frac{S}{N}\sqrt{\frac{2}{3}f_s}} \\ &= \sqrt{\frac{3}{8}}\frac{N \cdot P}{S \cdot \text{BW}} \\ \text{FOM}_\text{s} &\triangleq \frac{N \cdot P}{S \cdot \text{BW}} \end{aligned} \tag{3}$$

In (3), N is the noise power, P is the power consumption, S is the signal power, and BW is the bandwidth (BW) of the system. This figure of merit for a system is chosen since it captures all four important system parameters.

A conventional system is shown in Figure 6.

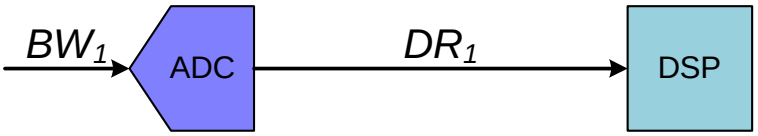


Figure 6: Conventional system composed of ADC and DSP.

In the above system, the total power consumption of the system can be calculated as follows.

$$\begin{aligned} P_{total,conv} &= \text{FOM}_\text{ADC} \cdot \text{BW}_1 \cdot \text{SNR}_1 + \text{FOM}_\text{DSP} \cdot \text{DR}_1 \cdot \text{SNR}_\text{F} \\ &= (\text{FOM}_\text{ADC} + \text{FOM}_\text{DSP}) \cdot \text{BW}_1 \cdot \text{SNR}_\text{F} \end{aligned}$$

BW_1 is the input signal bandwidth, SNR_1 is the input signal to noise ratio, SNR_F is the output signal to noise ratio, and DR_1 is the data rate for DSP. For the same bandwidth, the minimum data rate should be twice the bandwidth according to the Nyquist theorem, but here $\text{DR}_1 = \text{BW}_1$ is assumed since the factor of two can be transferred to FOM_DSP in a consistent way.

If we could have an analog signal processing (ASP) block with FOM_ASP which can compress bandwidth from BW_1 to BW_2, then a new system can be represented as Figure 7.

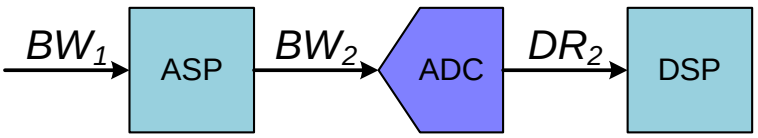


Figure 7: Proposed system composed of ASP, ADC and DSP.

In this system, the total power consumption is

$$\begin{aligned} P_{total,ASP} &= \mathrm{FOM_{ASP}} \cdot \mathrm{BW_1} \cdot \mathrm{SNR_1} + \mathrm{FOM_{ADC}} \cdot \mathrm{BW_2} \cdot \mathrm{SNR_2} + \mathrm{FOM_{DSP}} \cdot \mathrm{DR_2} \cdot \mathrm{SNR_F} \\ &= \mathrm{FOM_{ASP}} \cdot \mathrm{BW_1} \cdot \mathrm{SNR_F} \cdot \mathrm{NF_{ASP}} + \frac{1}{\mathrm{A_{BW}}} (\mathrm{FOM_{ADC}} + \mathrm{FOM_{DSP}}) \cdot \mathrm{BW_1} \cdot \mathrm{SNR_F} \end{aligned}$$

Therefore, to have the total power consumption of the proposed system to be lower than the total power consumption of the conventional system, following has to be satisfied.

$$\begin{aligned} & P_{total,conv} > P_{total,ASP} \\ & (\mathrm{FOM_{ADC}} + \mathrm{FOM_{DSP}}) \cdot \mathrm{BW_1} \cdot \mathrm{SNR_F} \\ & > \mathrm{FOM_{ASP}} \cdot \mathrm{BW_1} \cdot \mathrm{SNR_F} \cdot \mathrm{NF_{ASP}} + \frac{1}{\mathrm{A_{BW}}} (\mathrm{FOM_{ADC}} + \mathrm{FOM_{DSP}}) \cdot \mathrm{BW_1} \cdot \mathrm{SNR_F} \\ \therefore\ & \mathrm{FOM_{ASP}} < \frac{1}{\mathrm{NF_{ASP}}} \left(1 - \frac{1}{\mathrm{A_{BW}}}\right) (\mathrm{FOM_{ADC}} + \mathrm{FOM_{DSP}}) \end{aligned}$$

Let us assume a MIMO system of N as in Figure 8.

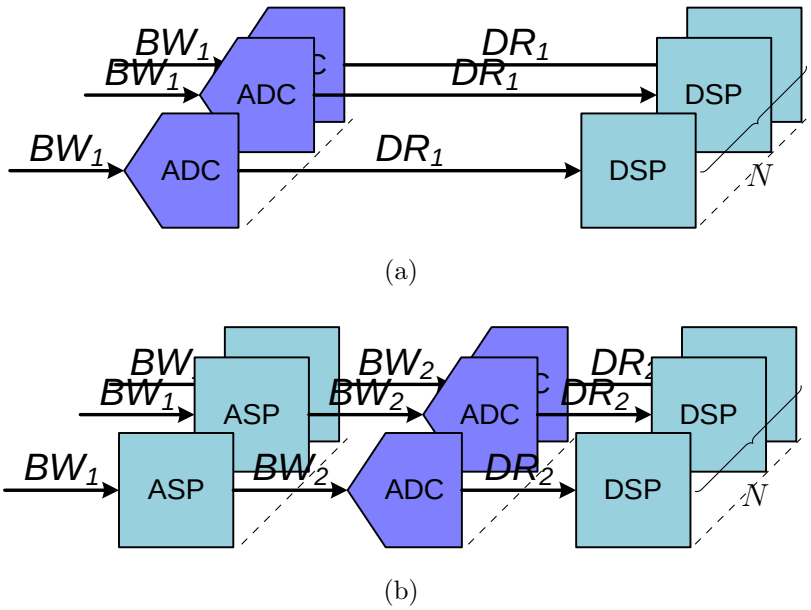


Figure 8: MIMO of N for (a) a conventional system, and (b) a proposed system.

Then the difference in power consumption becomes following.

$$P_{total,conv,N} - P_{total,ASP,N}$$
$$= N \cdot \left[\left(1 - \frac{1}{\mathrm{A_{BW}}} \right) (\mathrm{FOM_{ADC}} + \mathrm{FOM_{DSP}}) - \mathrm{FOM_{ASP}} \cdot \mathrm{NF_{ASP}} \right] \cdot \mathrm{BW_1} \cdot \mathrm{SNR_F}$$

If $\mathrm{A_{BW}}$ can be chosen as a large value, then the above equation can be approximated as follows.

$$P_{total,conv,N} - P_{total,ASP,N}$$
$$= N \cdot [(\mathrm{FOM_{ADC}} + \mathrm{FOM_{DSP}}) - \mathrm{FOM_{ASP}} \cdot \mathrm{NF_{ASP}}] \cdot \mathrm{BW_1} \cdot \mathrm{SNR_F}$$

Therefore, as far as $\mathrm{FOM_{ASP}}$ and $\mathrm{NF_{ASP}}$ can be chosen such that

$$\mathrm{FOM_{ADC}} + \mathrm{FOM_{DSP}} < \mathrm{FOM_{ASP}} \cdot \mathrm{NF_{ASP}}$$

is satisfied, the proposed system has an advantage over the conventional system.

CHAPTER III

CMOS INTEGRATED ANALOG PULSE COMPRESSOR (APC)

Either SAW devices or fast convolution processing has been used for conventional radar pulse compressors, but both solutions have significant drawbacks as discussed in Section 2.2. To overcome these drawbacks, an integrated APC for a MIMO radar has been developed with a 0.18–μm CMOS process using an arbitrary waveform generator, analog correlators, and analog-to-digital converters. In this chapter, the new APC will be discussed in detail. The proposed scheme not only has advantages over conventional methods but also adds additional flexibility to the MIMO system.

3.1 Introduction

Multiple-input multiple-output (MIMO) radars have been actively investigated as a next generation radar technology [2, 3]. However, a MIMO radar demands excessive signal processing power, and this is a major hurdle that must be overcome. A pulse compressor is an example of a key building blocks of a MIMO radar since a pulse compressor enables a radar to overcome fundamental trade-offs.

In radar, the target distance can be estimated by measuring $c\Delta t$ as depicted in Figure 9.

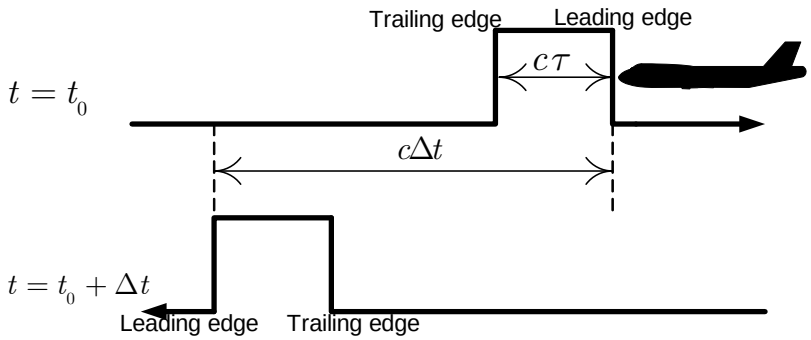


Figure 9: Target detection in a radar.

However, radar range resolution, pulse width, and average transmitted power have a trade-off since the range resolution is $\Delta R = c\tau/2$ and the average transmitted power is $P_{av} = P_t \tau f_r$, in which τ is the radar pulse width, c is the speed of light, P_t is the peak transmitted power, and f_r is the pulse repetition frequency. Therefore, the pulse width should be minimized for better (or smaller) range resolution, and the peak power of the radar has to be increased to maintain the same average power. A pulse compressor, which maintains high resolution of short pulses while allowing high average transmitted power of a long pulse, is commonly implemented by a matched filter (MF), but a pulse compressor requires significant signal processing power.

A digital signal processor (DSP)-based pulse compressor [14], commonly called as fast convolution processing (FCP) [30], shown in Figure 10 is very popular because of low cost and high performance of a modern DSP system.

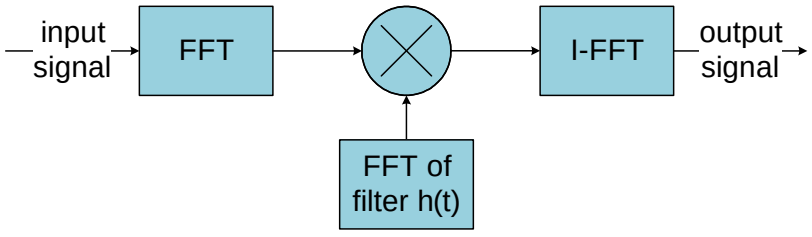


Figure 10: Fast Convolution Processing (FCP).

However, as discussed in Section 2.2, this approach or a digital finite impulse

response (FIR) filter implementation of an MF [16] consumes too much of power for itself since both FFT and IFFT are required or for the front-end ADC since a high sampling rate and a wide dynamic range are required. Other approaches such as the surface acoustic wave (SAW) device-based approach [13] do not have waveform flexibilities, or SOC is difficult since piezoelectric material is necessary.

An APC based on an analog MF has been suggested as a key block for the waveform diversity MIMO radar to overcome the problems discussed above because it can utilize complicated waveforms such as wavelets over traditional chirp signals [12, 31]. Unlike conventional approaches, a fully-integrated analog MF is implemented in the mixed-signal domain. Since this new implementation requires neither a FFT nor an IFFT, speed and power requirements for the ADC and the DSP can be relaxed. The system level evaluation shows that the 4×4 MIMO radar system based on the proposed approach consumes about six times less power than the 4×4 DSP-based MIMO radar system, and about four times less power than the DSP-based SISO radar system when tuned for a similar probability of detection performance [12]. Table 1 is the summary of results.

Table 1: Comparison of power consumption [12].

Item	Proposed	Comparison		
	ASP MIMO 4x4	DSP MIMO 4x4	DSP SISO	
Process	0.18 μm CMOS	90 nm CMOS (ASIC)	90 nm CMOS (ASIC)	65 nm CMOS (FPGA)
RF front-end (mW)	200	200	50	50
ADC Spec.	10 b 30 MS/s	11 b 80 MS/s	14 b 80 MS/s	14 b 80 MS/s
ADC (mW)	26.2	558.4	1117	1117
Matched Filter (mW)	196	1863.2	600	3000
Total (mW)	422.2	2621.6	1767	4167

The dynamic change of waveforms, which depends on the environment [32], is

possible in the analog MF owing to a random-access memory (RAM)-based arbitrary waveform generator (AWG). Since the transmitter needs to have a waveform generator, the AWG does not add significant overheads to the system. The AWG can also change the waveform duration during operation by simply changing addressing and clocking schemes, which enables multi-resolution, flexible waveform signal processing. This approach combines both the flexibility of the digital system and the simplicity of the analog system. This approach has been demonstrated by a multi-resolution spectrum sensing (MRSS) chip [33,34]. Unlike with the SAW-based MF, SOC integration is possible since the fabrication process is also fully CMOS compatible.

Even though various studies have suggested alternatives over a conventional MF (e.g., using capacitors as memory elements [17,18], using a charge transferring mechanism [19], an approach based on a floating-gate MOS [20], using a bank of digitally-controlled transconductors along with capacitors [21], current-mode operation [22], or a $\Sigma\Delta$ converter-based recycling integrator [23]), all of these approaches suffer from mismatches among circuit components or difficulties with long pulses. When the signal is restricted to a simple pulse, a similar approach to this work has been implemented for an ultra-wideband (UWB) application [35]. Since an MF is a quite general and powerful building block in wide range of modern signal processing applications, the analog MF for pulse compression could be extended to various radar signal processing functions. Furthermore, the proposed APC could be a viable approach for a very large scale phased array as in Figure 1.

3.2 Background

A filter whose impulse response is $h(t) = s^*(T-t)$, in which the signal $s(t)$ is assumed to be confined to the time interval $0 \leq t \leq T$, is called a matched filter to the signal $s(t)$. A matched filter attains a peak at $t = T$ [30,36]. The response of the MF $h(t)$

to the arbitrary input signal $s^i(t)$ at $t = T$ is

$$\begin{aligned} y_{t=T} &= s^i(t) * h(t)|_{t=T} \\ &= \int_{-\infty}^{\infty} s^i(\tau)h(T-\tau)d\tau \\ &= \int_{0}^{T} s^i(\tau)h(T-\tau)d\tau \\ &= \int_{0}^{T} s^i(\tau)s^*(\tau)d\tau. \end{aligned}$$

The matched filter maximizes the output signal-to-noise ratio (SNR) when signal $s(t)$ is corrupted by an additive white Gaussian noise (AWGN) process with power spectral density $\Phi(f) = \frac{1}{2}N_0$ (W/Hz), and the maximum output SNR is given as

$$SNR = \frac{2E}{N_0}, \tag{4}$$

where $E = \int_0^T |s(t)|^2 dt$ is the energy of the signal. Therefore, a long pulse compression time, which means large T with long $s(t)$, can increase the SNR, but it may limit the bandwidth of radar tracking in radar applications, especially with dynamic targets.

Let us consider $s^i(t) = s(t - \Delta t)$ as a time-shifted replica of $s(t)$ by Δt, and $s_k[n]$ as a sampled and delayed sequence of $s(t)$ by sampling frequency $1/T_s$ and the delay of integer k. In other words,

$$s_k[n] = \begin{cases} s((n-k)T_s), k \le n < k+N \\ 0, \text{ otherwise,} \end{cases}$$

where N is defined as

$$N \equiv \left\lfloor \frac{T}{T_s} \right\rfloor.$$

If a function $\tilde{y}(k)$ is defined as

$$\tilde{y}(k) \equiv \mathrm{Re} \int_{-\infty}^{\infty} s^i(\tau) s_k^*[\lfloor \tau/T_s \rfloor] d\tau, \tag{5}$$

and if an integer k can be found such that

$$\begin{aligned} k &= \lfloor (\tau + \Delta t)/T_s \rfloor - \lfloor \tau/T_s \rfloor \\ &\approx \left\lfloor \frac{\Delta t}{T_s} \right\rfloor, \end{aligned} \tag{6}$$

then

$$\begin{aligned}
\tilde{y}(k) &= \mathrm{Re}\int_{\Delta t}^{T+\Delta t} s(\tau-\Delta t)s_k^*[\lfloor \tau/T_s \rfloor]d\tau \\
&= \mathrm{Re}\int_0^T s(\tau)s_k^*[\lfloor (\tau+\Delta t)/T_s \rfloor]d\tau \\
&= \mathrm{Re}\int_0^T s(\tau)s_k^*[\lfloor \tau/T_s \rfloor + k]d\tau \\
&= \mathrm{Re}\int_0^T s(\tau)s^*(\lfloor \tau/T_s \rfloor T_s)d\tau \\
&\approx \mathrm{Re}\int_0^T s(\tau)s^*(\tau)d\tau \\
&= \int_0^T |s(t)|^2 dt \\
&= E,
\end{aligned}$$

which is the maximum from (4). Therefore, if the maximum of $\tilde{y}(k)$ with respect to k can be found, Δt can be estimated from (6) with the resolution of T_s. In turn, the target distance can be estimated as $\frac{ckT_s}{2}$ from k.

Furthermore, $\tilde{y}(k)$ is

$$\begin{aligned}
\tilde{y}(k) &= \mathrm{Re}\int_{-\infty}^{\infty} s^i(\tau)s_k^*[\lfloor \tau/T_s \rfloor]d\tau \\
&= \int_0^T \left(s_I^i(\tau)s_{k,I}[\lfloor \tau/T_s \rfloor] + s_Q^i(\tau)s_{k,Q}[\lfloor \tau/T_s \rfloor]\right)d\tau \\
&= \int_0^T s_I^i(\tau)s_{k,I}[\lfloor \tau/T_s \rfloor]d\tau \\
&\quad + \int_0^T s_Q^i(\tau)s_{k,Q}[\lfloor \tau/T_s \rfloor]d\tau,
\end{aligned} \tag{7}$$

where I and Q denote an in-phase and quadrature-phase component, respectively. signal $s(t)$ is already known since a radar has to transmit this signal. Therefore, by shifting the sampled $s(t)$ by an appropriate amount, $s_k[n]$ can be constructed, and (7) can be calculated by

1. Multiplying an input signal with $s_k[n]$

2. Integrating over time $0 \leq t \leq T$

3. Sampling the integrator outputs at time T

4. Adding sampled integrator outputs of the I path and the Q path

The input signal $s^i(t)$ is not sampled, while the known sampled sequence $s_k[n]$ of the transmitted signal $s(t)$ is used, so a high-speed ADC is not required. Moreover, instead of the input signal, the reference signal shifts. The reference code-shifting digital MF [16] uses a similar scheme.

3.3 Architecture

3.3.1 Block Diagram

A block diagram of an APC is shown in Figure 11 as a building block for a MIMO radar.

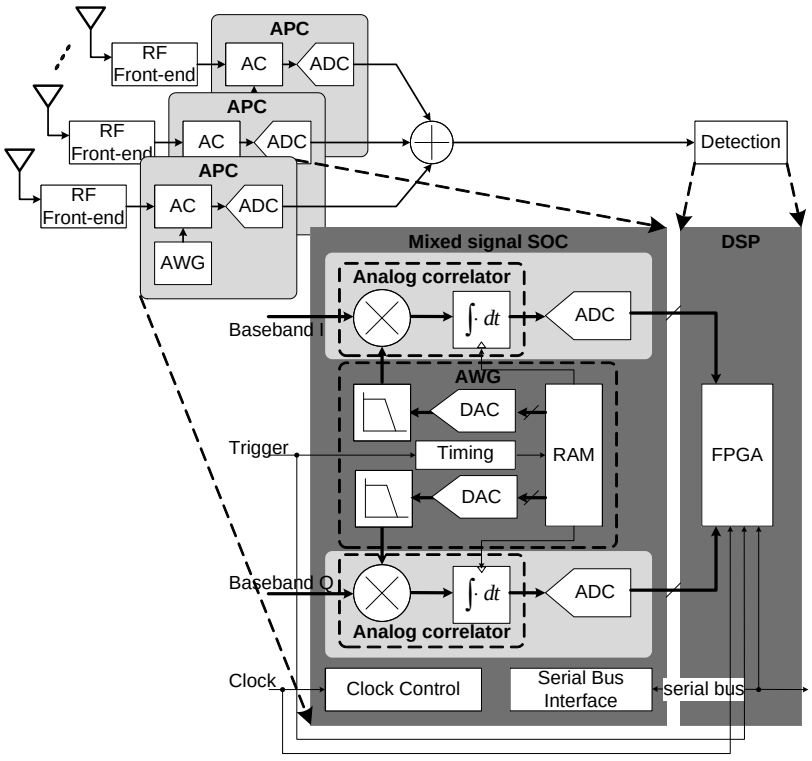


Figure 11: MIMO radar architecture and analog pulse compressor (APC) block diagram.

$s^i(t)$ and $s_k[n]$ of (5) correspond to an input signal and an AWG signal, respectively. The baseband I and Q signals are received, and the correlation is performed by multiplying these signals with the signals generated by the AWG, and then integrated. In order to make the waveforms for the separate I and Q paths, the AWG is composed of 22-bit RAM (11-bit for each path), four (two for each path to generate differential signals) 11-bit digital-to-analog converters (DACs), and two low-pass filters (LPFs). The maximum signal length is 1,024 since the RAM is configured as four banks of 256×22 bits. The RAM stores a digitized signal, and DACs convert digitized signals to analog signals. The 22-bit data of the RAM are read by two latch blocks for each I and Q separately, which enable complementary and synchronized outputs for the DACs. The LPF eliminates the digital clock spurs and out-of-band frequency components, and the LPF is implemented as a 6th-order Chebyshev type-II configuration. The bandwidth of the LPF is tunable from 1.67 MHz to 5.18 MHz. Then, the final outputs of the analog correlator are sampled by two 9-bit pipeline ADCs and sent to an external FPGA for further signal processing. The on-chip serial bus interface configures these functionalities, and the FPGA is integrated on a test board to emulate a DSP block. Differential signaling has been used throughout the circuit to reduce even-order harmonics and to increase the power supply rejection ratio (PSRR) and immunity from noise. The following is a summary of each block, and the details of which will be explained in Section 3.5.

- AWG
  - Maximum clock frequency: 38.4 MHz
  - RAM: maximum data length of 1024 points with two 11-bit data for separate I and Q signals
  - DAC: 11-bit R/2R configuration
  - LPF: 6th order Chebyshev type-II with tunable bandwidth

  - Waveform duration: ÷1, ÷2
  - Adjustable delay

- Analog correlator
  - Analog multiplier: up to 500 $\mathrm{mV_{pp-diff}}$ input signal
  - Integrator: R/C controllable and resettable
  - DC offset cancellation: 6-bit current DAC

- ADC
  - Two 9-bit pipeline ADCs for separate I and Q paths
  - Maximum sampling frequency: 30 MHz
  - Maximum input signal range: 2.8 $\mathrm{V_{pp-diff}}$

- Clock control
  - Input clock frequency: 38.4 MHz
  - Clock divider (separate for AWG and ADC): ÷1, ÷2, ÷4, ÷8

- Serial bus interface
  - Control registers: 18×8 bits

3.3.2 Timing Control

The signal was assumed to be confined in the time interval $0 \leq t \leq T$ in Section 3.2. Let us assume f_r is pulse repetition frequency. If the entire time period of $1/f_r$ is scanned by increments of k by 1, then the total time to find Δt will be

$$\begin{aligned} T_{total} &= \frac{1}{f_r} \times (iteration) \\ &\approx \frac{1}{f_r} \frac{1}{f_r T_s}, \end{aligned} \tag{8}$$

since $|k|$ has to scan from 0 to $\lfloor 1/(f_r T_s) \rfloor$ to cover an entire period. In this situation, considerable time could be taken to scan an entire time period.

In the proposed APC, the time period of $1/f_r$ is scanned while the ADCs sample the signals synchronously with the repeating AWG signals. This concept is illustrated in the system timing diagram as in Figure 12 assuming the chirp signals as the input and reference signals. The input return signals from the targets are assumed to be present at $\Delta t_1 = T$ and $\Delta t_2 = (3 + 1/4)T$, respectively. Even though both the I and Q signals are considered for the correlator output shown, only the I-path signals are shown for clarity.

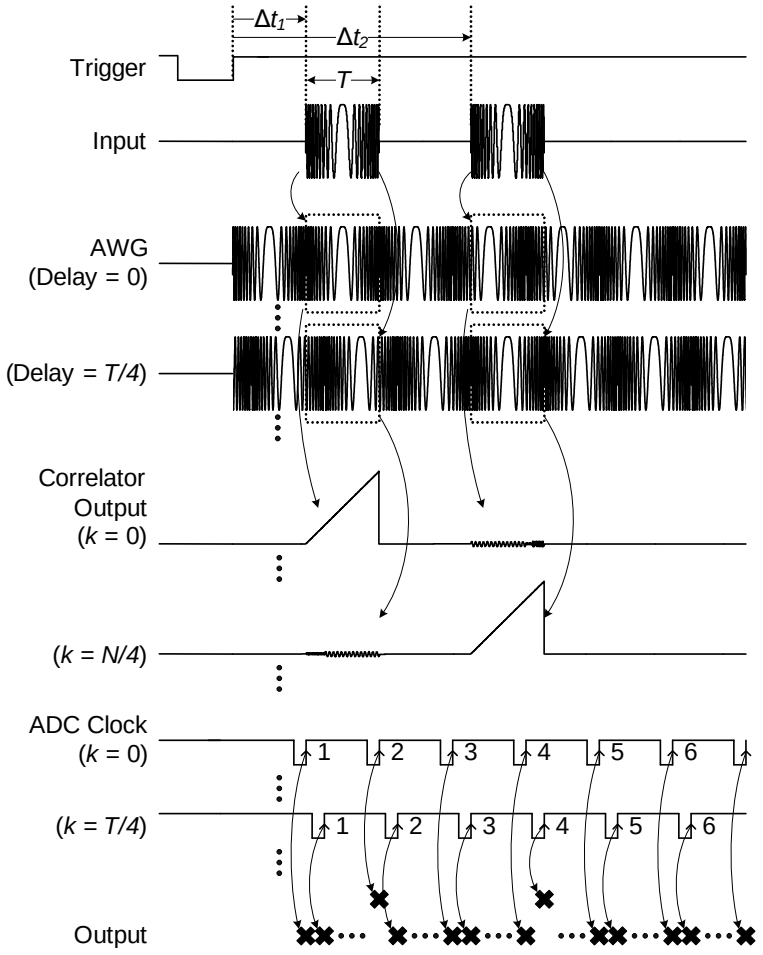


Figure 12: System timing diagram.

The trigger input is synchronized with the transmission of the signal. When the

trigger comes in, then the AWG starts with a certain delay parameter k, which can be controlled over the serial interface. Since the AWG is RAM based, an AWG output synchronized with the trigger starting at arbitrary k with a range of $0 \leq k < N$ can be generated as will be shown later in Subsection 3.5.1. Then, this delayed AWG signal is repeated until the next trigger comes in. The integrator output is sampled by the ADC at the end of period N right before the integrator is reset for the next integration cycle.

The first case in Figure 12 is when $k = 0$. Since the signal return from the first target corresponds to the second sampling instance of the ADC, the second sample from the ADC will return the largest correlation value. However, the fourth sample, whose value is exaggerated about four-fold to highlight the difference with zero values in the figure, will be much smaller since the correlation value is small due to the time lag between the input signal and the reference signal, and all other samples will be zero. The second case in Figure 12 is when $k = N/4$. In this case, the second sample from the ADC will yield a small correlation value unlike the first case due to the time lag, while the fourth sample will yield the highest correlation value, and all other samples will be zero.

Therefore, in the proposed APC, the total time to find Δt for multiple targets with the increment of k by 1 is

$$\begin{aligned} T_{total} &= \frac{1}{f_r} \times (iteration) \\ &= \frac{N}{f_r}. \end{aligned} \tag{9}$$

Unlike (8), T_{total} is only inversely proportional to f_r in the above equation except for the case when duty cycle approaches one, in other words $1/f_r \rightarrow NT_s$, where (9) approaches (8). Also, this analysis shows that careful trade-offs among pulse length N, sampling time T_s, and pulse repetition frequency f_r are required. However, (9) is the worst case estimation. The average T_{total} could be much lower with a simple binary search algorithm such as searching with $k \gg 1$ first and only searching the interval

in which the signal return is higher than the threshold with half of the previous k.

3.4 System Simulations

Before a real circuit is implemented, extensive simulations have been performed to investigate the system performance and to specify each block in detail. A chirp signal is used as a reference signal with the following simulation conditions.

1. Radar
    - Pulse repetition frequency (PRF): 10 kHz
    - Target positions: 1 km, 3 km, 10 km with the same radar cross section (RCS)
    - SNR: 5 dB with respect to white Gaussian noise
    - Assume coherent detection
    - Path loss is not considered
2. AWG
    - Clock frequency: 19.2 MHz
    - RAM: data length of 512 points
    - DAC resolution: 11 bit
    - LPF: Butterworth 6th order, cut-off at 6 MHz
3. Integrator
    - Dead time: 10 points
    - Dominant pole: 1 kHz

MATLAB[1] has been used for the simulation. Figure 13 shows the transmitted pulse, and Figure 14 shows received echoes before compression. The top graph of

[1]Product of The MathWorks Inc., Natick, MA. [Online]. Available: www.mathworks.com

Figure 13 is the pulse in the time domain, and the bottom graph of Figure 13 is the pulse in the frequency domain. The cut-off of LPF can be verified to be sufficiently high from this figure.

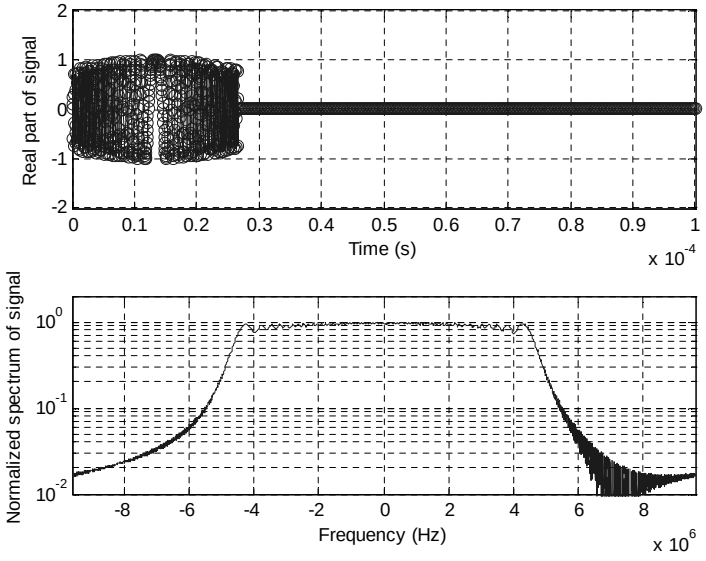


Figure 13: Transmitted pulse in a time domain and a frequency domain.

It is clear from the top graph of Figure 14 that two echoes centered at

$$1\,\mathrm{km} = \frac{2 \times 1\,\mathrm{km}}{c} + \frac{512}{2 \times 19.2\,\mathrm{MHz}} = 20.0\,\mu\mathrm{s}$$

and

$$3\,\mathrm{km} = \frac{2 \times 3\,\mathrm{km}}{c} + \frac{512}{2 \times 19.2\,\mathrm{MHz}} = 33.3\,\mu\mathrm{s}$$

overlap, so it is difficult to discern echoes separately when signals are received together, as in the bottom graph of Figure 14. Also, the signal is significantly corrupted by noise.

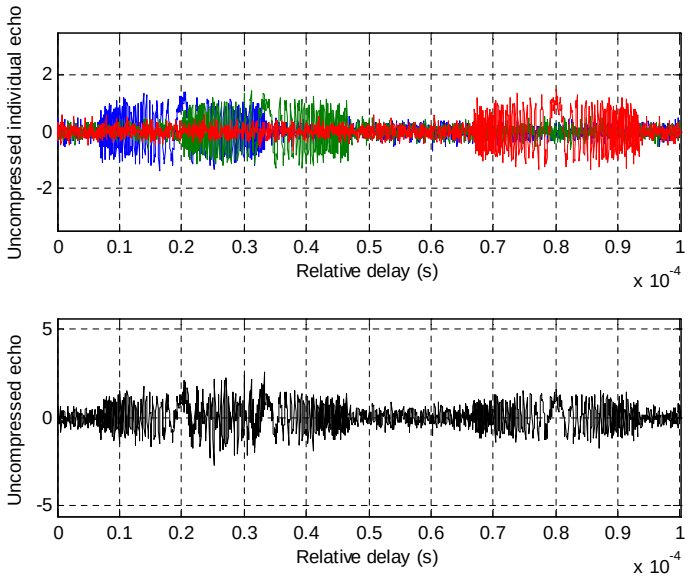


Figure 14: Received individual echoes and the combined signal.

Figure 15 shows reconstructed echoes by pulse compression. All target echoes are clearly distinguishable, and the signal is at least 10 dB higher than the noise level.

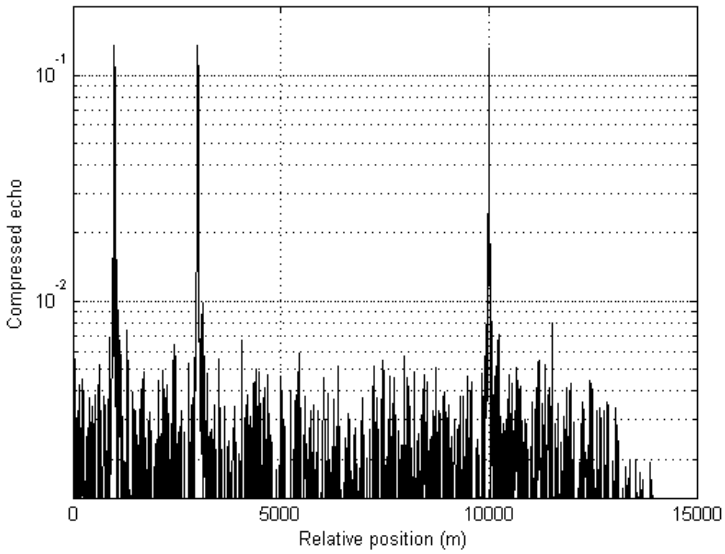
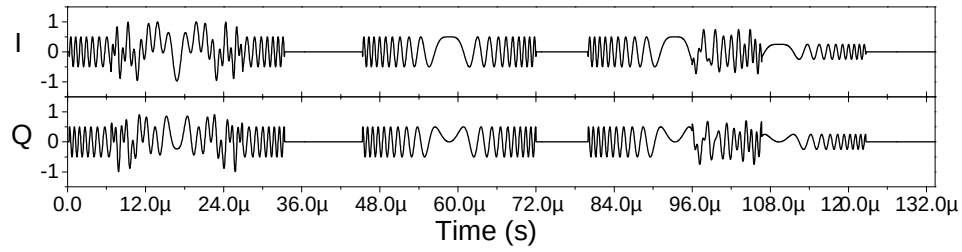
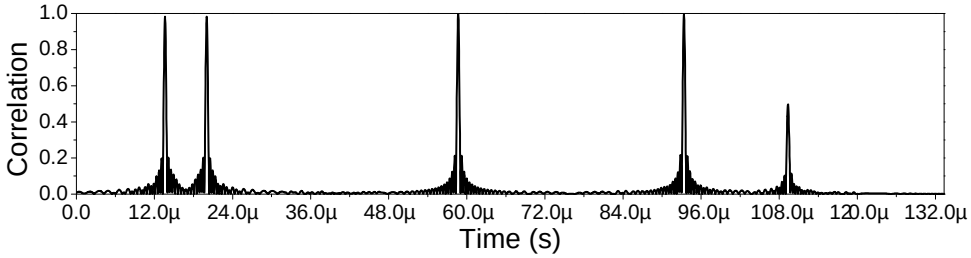


Figure 15: Reconstructed echoes of the chirp signal.

Figure 16(a) shows the case when 5 chirp signals overlap with different amplitudes and timing, and Figure 16(b) shows the response of the simulated MF. It clearly shows five distinctive waveforms separated with correct amplitudes.



(a)



(b)

Figure 16: (a) Input signals I and Q, and (b) a simulated matched filter response of multiple chirp signals.

As an initial effort to extend this matched filter to the waveform diversity, Daubechies 8th order wavelet has been used instead of the chirp signal, with similar simulation conditions (See Figure 17).

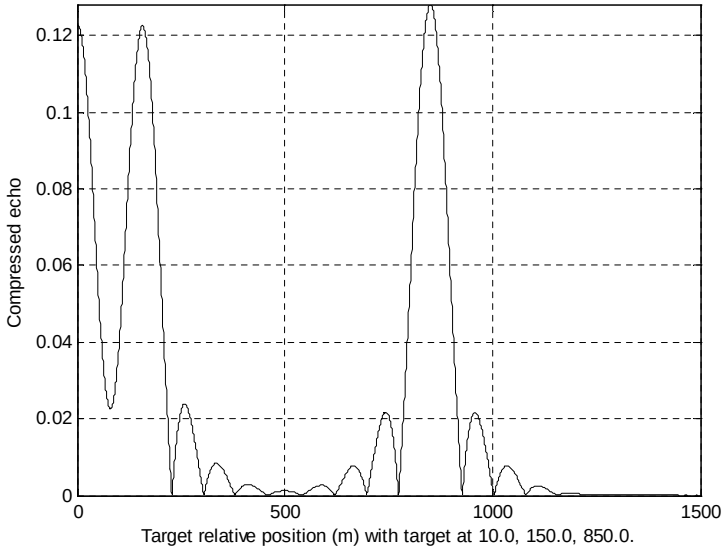


Figure 17: Reconstructed echoes of wavelets.

Even though this simulation result shows inferior performance of the wavelet over that of the chirp signal, active investigation is underway to exploit the orthogonality and the multi-resolution feature of wavelets.

3.5 Building Blocks

3.5.1 Arbitrary Waveform Generator (AWG)

Figure 18 shows a block diagram of the RAM and address generator in the AWG.

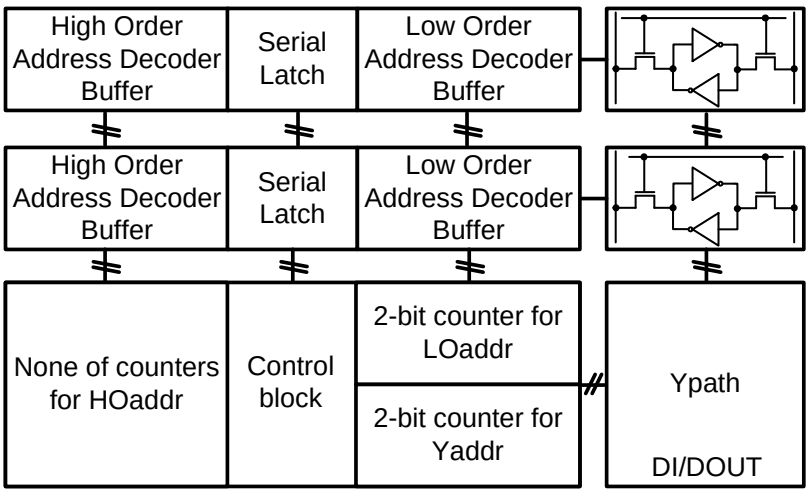


Figure 18: RAM and address generator of AWG.

RAM continuously accesses the digital data stored to generate the waveform sequentially from the AWG by the addresses generated in the address generator block. Among the total 10-bit addresses, 2-bit low-order addresses (LOaddr) are generated by a 2-bit counter, and 6-bit high-order addresses (HOaddr) for x-decoders are generated in the embedded serial latch to reduce the power consumption in the address buffer blocks. The other 2-bit y-addresses are generated by an internal 2-bit counter. In this way, a total of 1,024 addresses are accessible with reduced power consumption. A clock frequency (f_{CLK}) and duration control bits ($Resol$) control the duration of the waveform. The digitally-controlled, multi-resolution radar pulse compression technique can be implemented by adapting this waveform flexibility.

Figure 19 shows the timing diagram of the AWG when external HOaddr is 100000_2 and LOaddr is 10_2, so the address is $10000010_2 = 130_{10}$. Above external address is loaded into the internal address generator of the AWG when the AWG_EN signal is enabled to a high state, and the internal address is incremented at every clock afterwards. The AWG repeats the waveform automatically after one period of the waveform is generated.

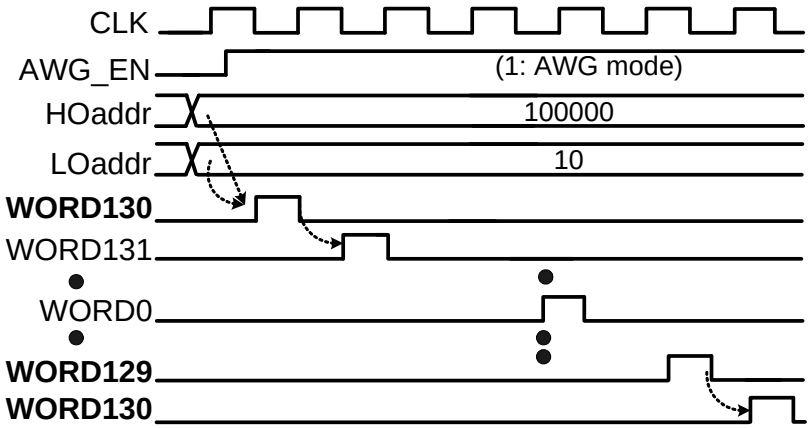


Figure 19: AWG timing diagram.

Figure 20 demonstrates the multi-resolution feature of the AWG when chirp signals are used for both the I and Q channels. For example, if $f_{CLK} = 4.8\,\text{MHz}$ and $Resol = \div 1$, the time period T is $T = 1024/4.8\,\text{MHz} \approx 223\,\mu\text{s}$. By changing the clock divisor and AWG duration control bits, both f_{CLK} and $Resol$ can be changed through the serial bus interface, respectively. The oscilloscope time scale per division is fixed to $20\,\mu\text{s}$ for all cases in Figure 20.

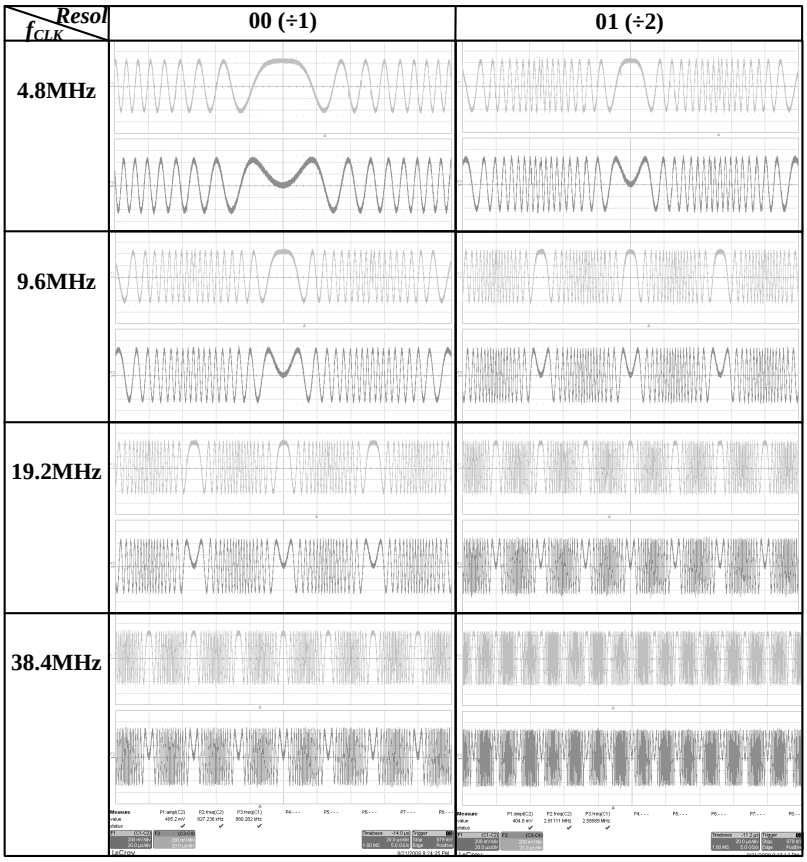


Figure 20: Measurement of chirp I, Q signals generation in multi-resolution.

The radar pulse compression uses chirp signals extensively since they can be generated easily [5]. Therefore, a chirp signal is chosen as a standard signal in this work, but the AWG allows other waveforms such as wavelets. As an illustration of waveform diversity, Figure 21 presents the measurement results for a Daubechies 8th-order wavelet with signal frequency $1/T$ at 37.5 kHz ($f_{CLK} = 38.4$ MHz, $Resol = \div 1$).

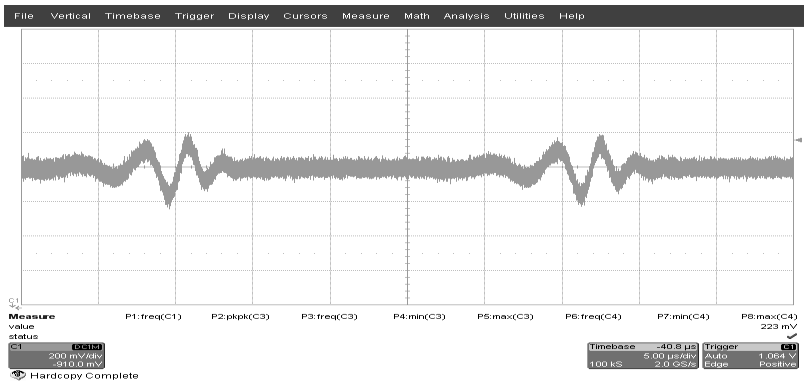
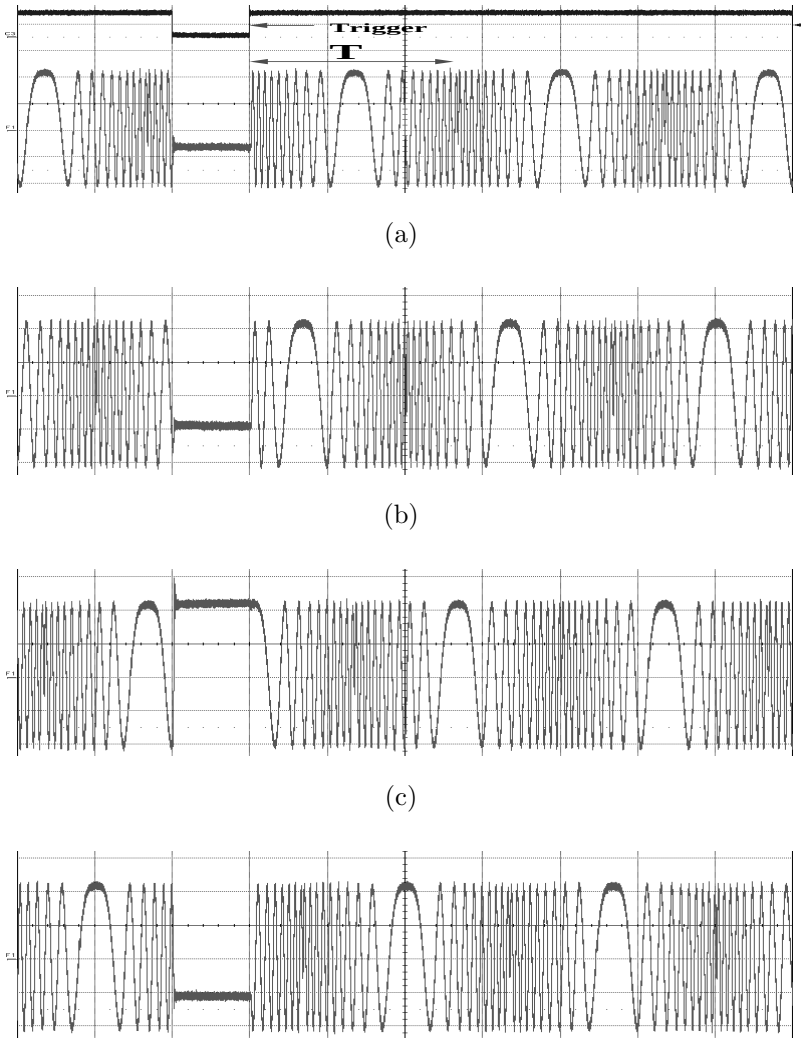


Figure 21: Measurement results for the Daubechies wavelets.

In the pulse compression, identifying the distance requires the starting point of the waveform to be controlled and adjusted digitally, as explained in Section 3.3.2. Figure 22 shows the measurement results of the arbitrary starting point characteristic of the AWG. In this figure, AWG generates chirp waveforms with delays of 0, 1/4, 2/4, and $3/4\,T$ of the entire waveform period T with respect to the external trigger signal. The step resolution of the waveform delay is $T/1024$.



(a)

(b)

(c)

(d)

Figure 22: Measurement results of arbitrary starting chirp waveforms with delay of (a) $0\,T$, (b) $1/4\,T$, (c) $1/2\,T$, and (d) $3/4\,T$.

3.5.2 Analog Correlator

The analog correlator consists of a multiplier and an integrator for correlating the input baseband signal and the signal generated from the AWG. Figure 23 shows the architecture of the analog correlator [33].

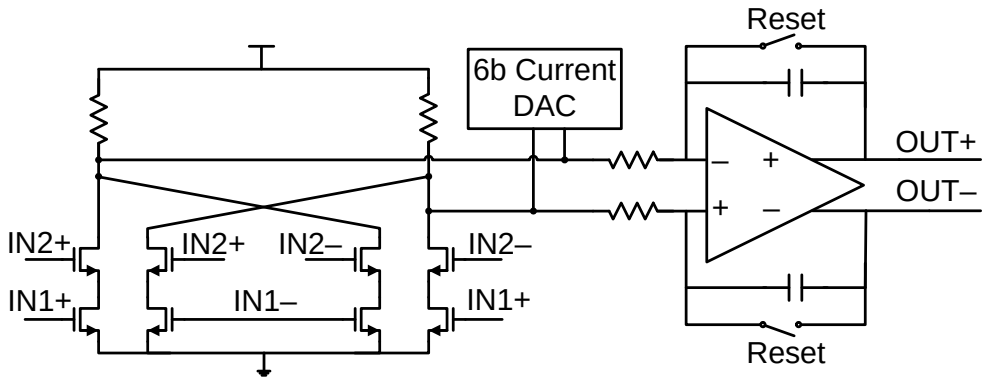


Figure 23: Analog correlator schematic.

Bottom transistors are biased at the linear region, and top transistors are source followers to deliver input voltages at the drains of bottom transistors. The 6-bit current DAC is included to mitigate the undesirable DC offset by injecting a small amount of bias current to the input of the integrator. The amount of bias current is controlled by serial interface. At the end of every pulse, a reset signal from the AWG initializes the integrator for the subsequent correlation operation. This reset signal is also available to outside so that the FPGA can sample ADC outputs with appropriate timing. The gain and the dominant pole position of the integrator can be adjusted through the on-chip serial bus interface.

The correlation operation is shown in Figure 24 with the measurement results when the chirp signal from the AWG is synchronized with the input signal.

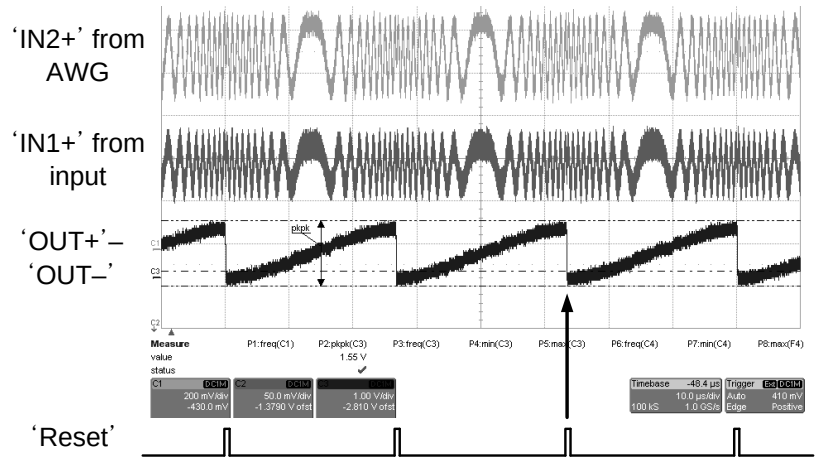


Figure 24: Analog correlator time-domain measurement results.

The output results are high since two signals are aligned. The following ADC captures the buffered correlation output for further signal processing in a digital domain. Then, the AWG resets the integrator automatically for the subsequent correlation operation on every cycle.

3.5.3 Analog-to-Digital Converter (ADC)

Figure 25 shows the block diagram of a low-power differential pipeline ADC. The maximum sampling frequency is chosen as 30 MHz with enough margins for future extensions.

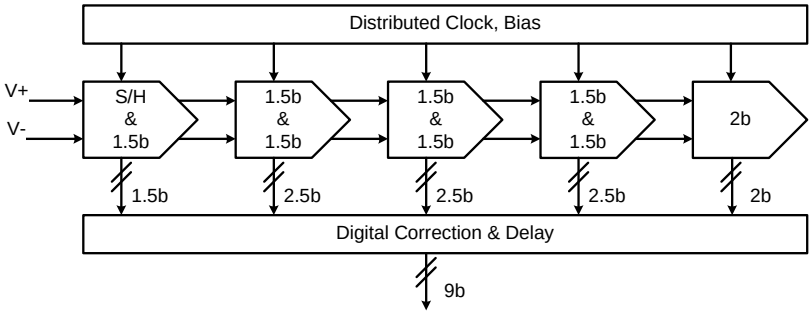


Figure 25: ADC block diagram.

The first block is a sample-and-hold (S/H) stage, and eight pipeline stages follow. A digital correction block merges all of the digital outputs and generates the final 9-bit

output. The final output is available to the outside of the chip through a multiplexer. Each neighboring pair of stages, including the S/H stage, share a common op amp for power reduction, so only a total of four op amps are required. To increase an output dynamic range, two-stage op amps with a single-stack output stage are used, and dynamic comparators with complementary inputs are used to increase an input dynamic range, as will described in Chapter 4. Figure 26 shows the FFT results of the ADC measurement.

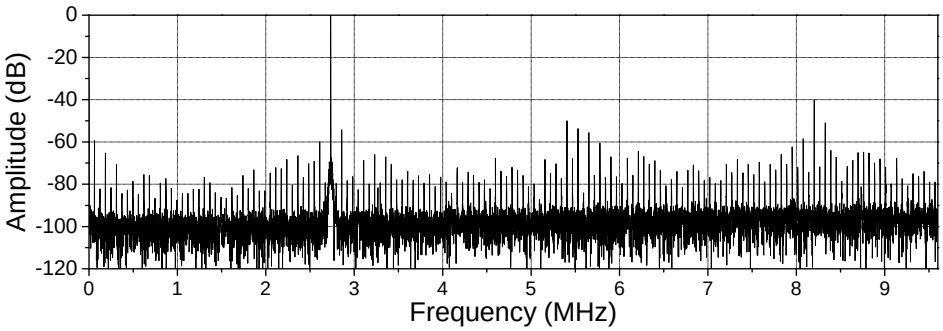


Figure 26: Measured output FFT spectrum of the ADC.

The signal generator clock is synchronized to the ADC clock. A test input frequency of 2.7340 MHz was chosen for coherent sampling as it prevents spectral leakage without window [37]. With an input signal level of 2.8 $V_{pp-diff}$, the effective number of bits (ENOB) was 7.02 b from 16,384-point FFT at 19.2 MS/s. In the above operating conditions, power consumption was 16.2 mW. The figure of merit (FOM), defined as $P/(2^{ENOB} \cdot f_s)$ [9] is 6.50 pJ/conversion-step, in which P is the power consumption and f_s is the sampling frequency.

3.6 System Evaluation

The APC was fabricated in a 0.18-μm CMOS technology process. The die size is 3.13 mm $\times$ 1.81 mm, and a die micrograph is shown in Figure 27. All the blocks and pads are positioned carefully to ensure signal integrity and to minimize the coupling effects on analog signals from digital signals.

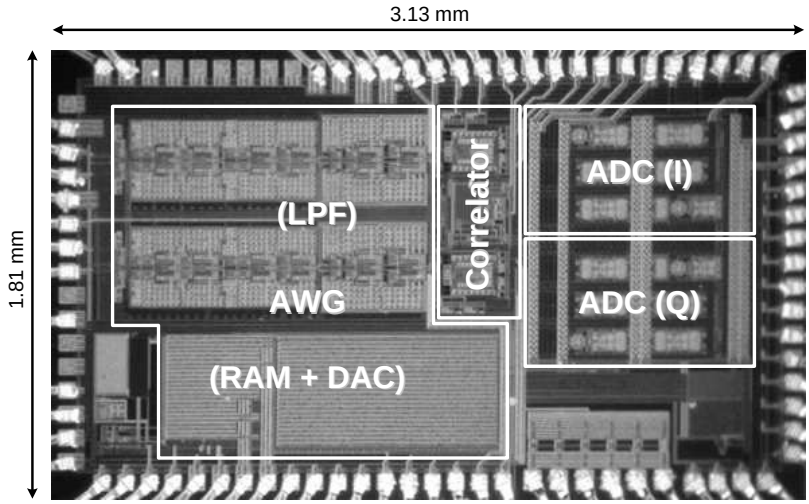


Figure 27: Die micrograph.

The AWG was loaded with the 2×11-bit chirp signal, and separate input signals for I and Q paths are injected from an external arbitrary function generator. The final digital data from the ADC at 1.2 MS/s were gathered by the FPGA and sent to a computer. The ADC sampling frequency was reduced from its maximum to 1.2 MS/s to save power since integrator outputs do not require a high sampling frequency. As discussed in Section 3.2, the ADC sampling frequency can be lowered even further to 38.4 MHz/1024=37.5 kHz, but oversampling was performed to ensure that the integrator output timing was aligned correctly relative to the reset signal. However, only one ADC output per each integration cycle right before the reset was used for the analysis. Therefore, the power consumption of the ADC can be lowered even further with a lower sampling frequency in the future. As the timing diagram shows in Figure 12, the ADC outputs were gathered for multiple samples during the time period of $1/f_r$. These steps were repeated while the FPGA shifts the starting point(k from Section 3.3.2) of the AWG . Figure 28 shows the test setup environments with the custom designed printed circuit board (PCB).

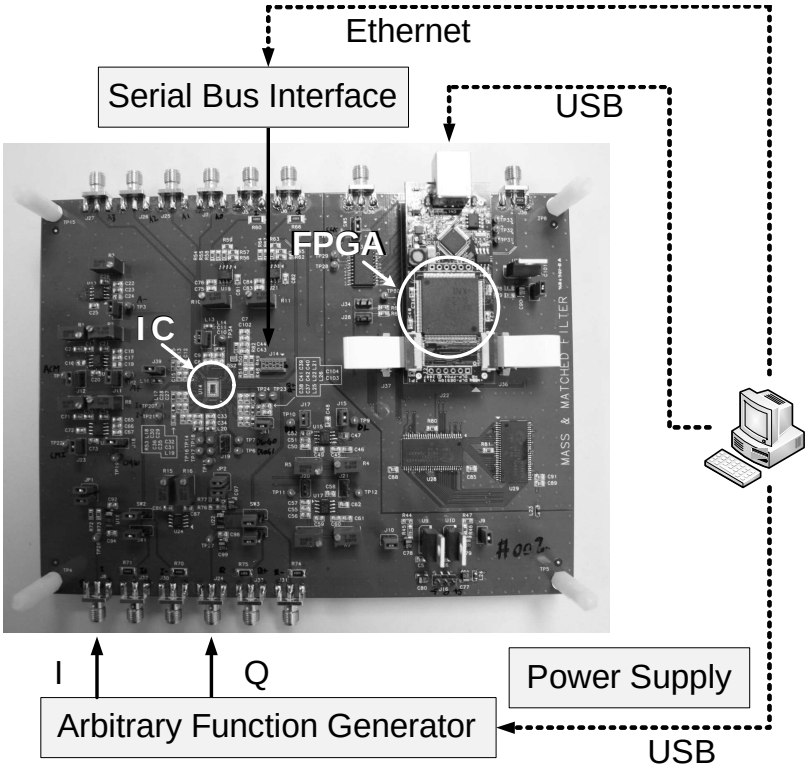


Figure 28: Test environments.

Figure 29 compares the measured matched filter response of a chirp signal with that of a simulation.

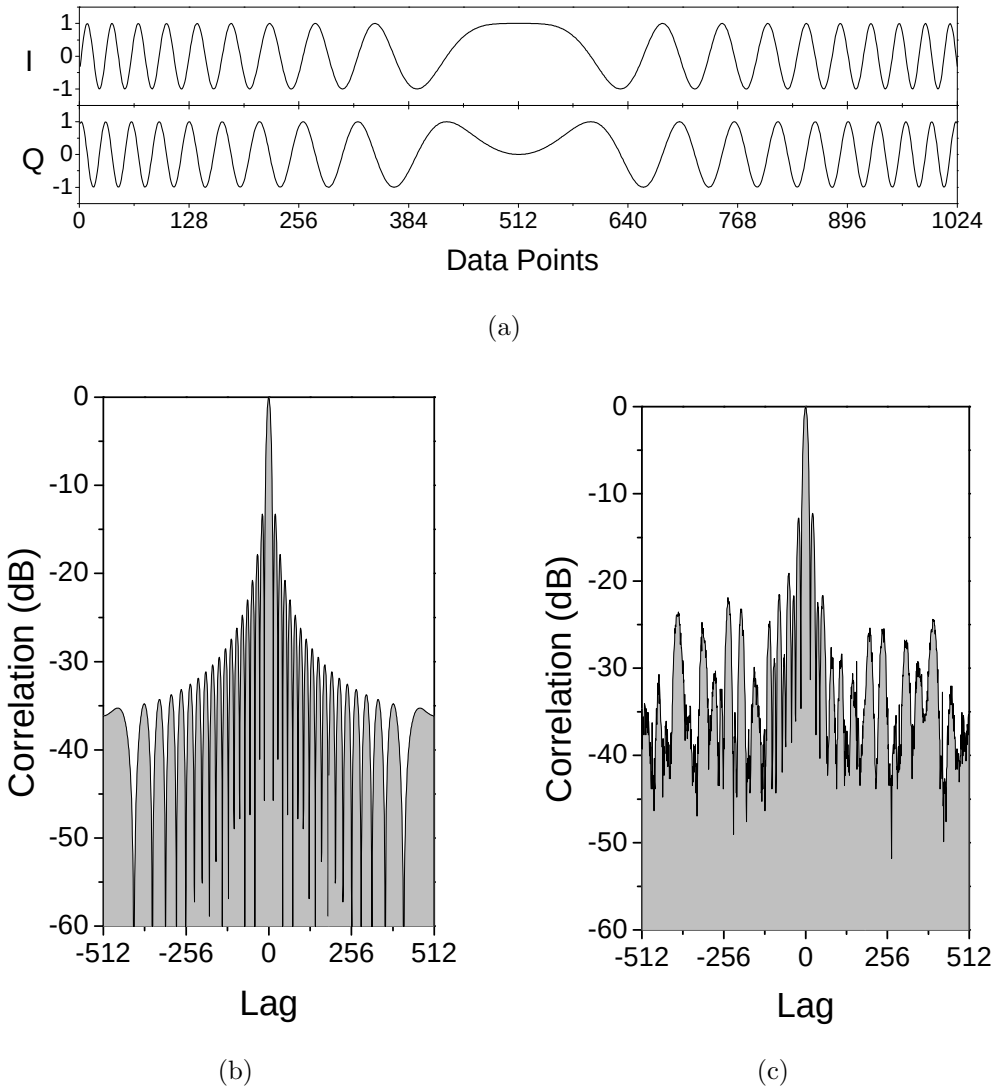


Figure 29: (a) Input signals I and Q in a time domain, (b) a simulated matched filter response, and (c) a measured matched filter response (average of 10) of a chirp signal.

Figure 29(a) shows the time domain waveform of the chirp signal used for these measurements. This chirp signal has a 3 dB bandwidth of about 1.3 MHz with $f_{CLK} =$ 38.4 MHz and $Resol = \div 1$. Figure 29(b) shows the simulated matched filter response of the above chirp signal, and Figure 29(c) shows the experimentally obtained response by incrementing k by 1 each time. For convenience, the x-axis was shifted by a constant offset to match the measured response to the ideal one, and the sampled data were normalized to the maximum sampled value. For this experiment, the

system clock was not synchronized with the clock of an external arbitrary function generator.

Above measurement shows that a noise dominates below a ∼-35 dB level. The following formulas are used to estimate an SNR and a dynamic range (DR) for the whole system.

$$\mathrm{SNR\,(dB)} \equiv 10\log_{10}\left(\frac{\sum_{k=-m}^{m}|\tilde{y}(k)|^2}{\sum_{k=-\frac{N}{2}}^{-m-1}|\tilde{y}(k)|^2+\sum_{k=m+1}^{\frac{N}{2}-1}|\tilde{y}(k)|^2}\right), \tag{10}$$

$$\mathrm{DR\,(dB)} \equiv 10\log_{10}\left(\frac{\max_{k=-m}^{m}|\tilde{y}(k)|^2}{\max\left(\max_{k=-\frac{N}{2}}^{-m-1}|\tilde{y}(k)|^2,\max_{k=m+1}^{\frac{N}{2}-1}|\tilde{y}(k)|^2\right)}\right), \tag{11}$$

where m is determined by the range of bins occupied by the signal. This approach is similar to spectral estimation from FFT in ADC characterization [38]. Since the simulation indicates that the main lobe occupies $-14 \le k \le 14$, $m = 14$ was used with $N = 1024$. The measurement results of ten trials are shown in Figure 30. The maximum SNR calculated as (10) was 8.88 dB, and the maximum DR calculated as (11) was 12.53 dB. These values include all the noise and dynamic ranges of the entire system, i.e., degradation from the AWG, the analog correlator, and the ADC. The mean values of the SNR and the DR values are derived from the following formulas.

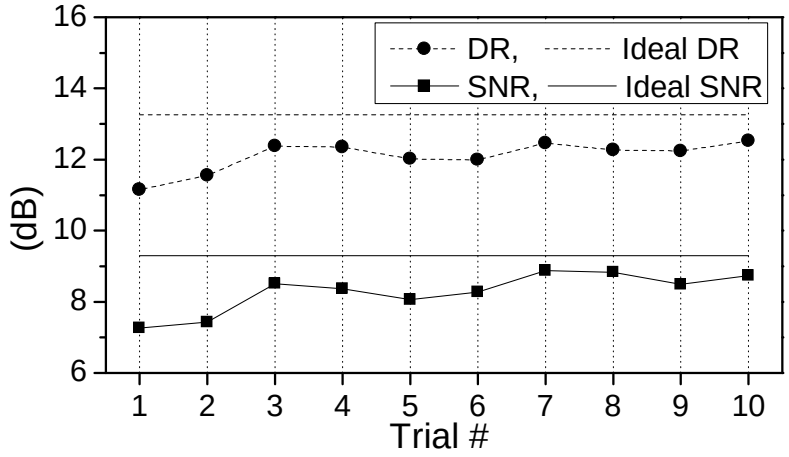


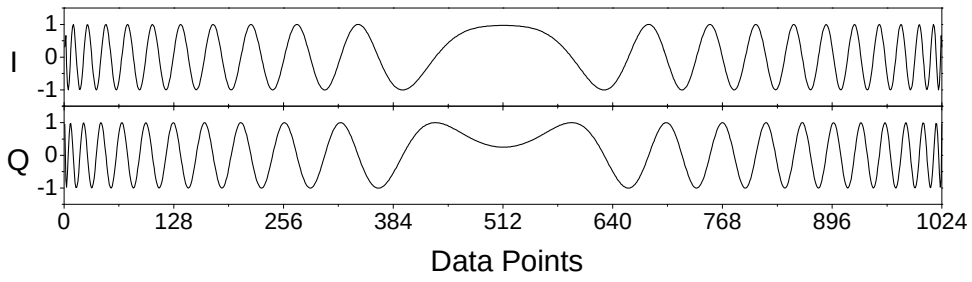
Figure 30: Multiple trials with a chirp signal.

$$\mathrm{SNR}_{\mathrm{avg}}\,(\mathrm{dB}) \equiv 10\log_{10}\left(\frac{\sum_{l=1}^{M}\sum_{k=-m}^{m}|\tilde{y}_l(k)|^2}{\sum_{l=1}^{M}\left(\sum_{k=-\frac{N}{2}}^{-m-1}|\tilde{y}_l(k)|^2+\sum_{k=m+1}^{\frac{N}{2}-1}|\tilde{y}_l(k)|^2\right)}\right) \tag{12}$$

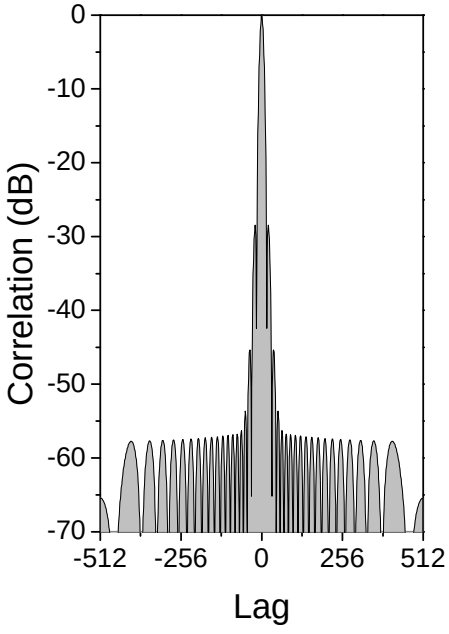
$$\mathrm{DR}_{\mathrm{avg}}\,(\mathrm{dB}) \equiv 10\log_{10}\left(\frac{\sum_{l=1}^{M}\max_{k=-m}^{m}|\tilde{y}(k)|^2}{\sum_{l=1}^{M}\max\left(\max_{k=-\frac{N}{2}}^{-m-1}|\tilde{y}_l(k)|^2,\max_{k=m+1}^{\frac{N}{2}-1}|\tilde{y}_l(k)|^2\right)}\right) \tag{13}$$

The average SNR calculated from (12) was 8.26 dB, and the average DR calculated from (13) was 12.08 dB.

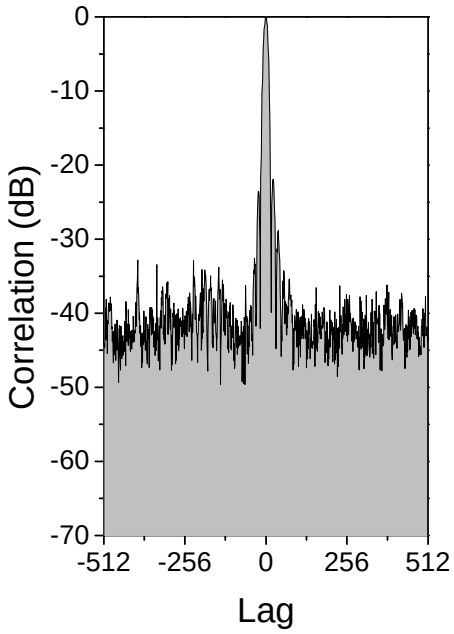
Since the ideal SNR and the DR for a chirp signal calculated by (10) and (11) are only 9.30 dB and 13.26 dB, respectively, the system performance can not be better than these values. Therefore, a nonlinear frequency modulation (NLFM) signal was used to estimate system performance more accurately. The proposed APC can easily accommodate a complicated waveform such as an NLFM owing to the AWG. Figure 31 compares the measured matched filter response of an NLFM with that of a simulation.



(a)



(b)



(c)

Figure 31: (a) Input signals I and Q in a time domain, (b) a simulated matched filter response, and (c) a measured matched filter response (average of 10) of an NLFM signal.

Figure 31(a) shows the time domain waveform of an NLFM signal [39] with the phase modulation as

$$\theta(t) = \frac{\pi\beta_L}{T}t^2 - \frac{\pi\beta_C T}{2}\sqrt{1-4\frac{t^2}{T^2}}, |t| \leq \frac{T}{2}$$

with $\beta_L \approx 1.86\,\mathrm{MHz}$, and $\beta_C \approx 744\,\mathrm{kHz}$. Since the main lobe occupies $-16 \leq k \leq 16$ from the simulation, the ideal SNR and DR for the NLFM signal calculated by

(10) and (11) using $m = 16$ are 27.2 dB and 28.5 dB, respectively. Figure 31(b) and Figure 31(c) show the simulated matched filter response and the experimentally obtained response with the same experimental conditions as a chirp signal. The difference between the ideal response and the measured response is more pronounced than a chirp signal case. The high baseline could be mainly due to DC offsets of the integrators. Figure 32 shows the measurement results from ten trials. The maximum SNR and the maximum DR calculated as (10) and (11) were 18.96 dB and 22.69 dB, respectively, and the average SNR and the average DR calculated as (12) and (13) were 18.09 dB and 20.54 dB, respectively. Both numbers are higher than numbers from a simple chirp signal.

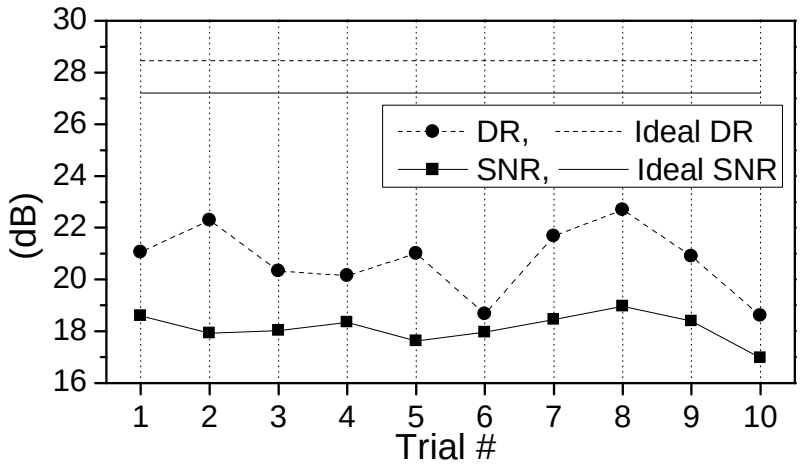


Figure 32: Multiple trials with an NLFM signal.

A chirp signal of period T followed by an empty interval of T was applied to the input for an SNR and a DR estimation of the correlator alone. The output signal was measured as an integration value at the chirp signal interval with the lag for the maximum correlation value while the output noise was measured as an integration value at the empty interval. Figure 33 compares the measured signal and the noise according to the different input level. The input signal level of 5 $\mathrm{mV_{pp-diff}}$ is normalized to 0 dB, and the output is normalized to 0 dB at the maximum output

value. The input amplitudes were increased by 0.2 dB increment.

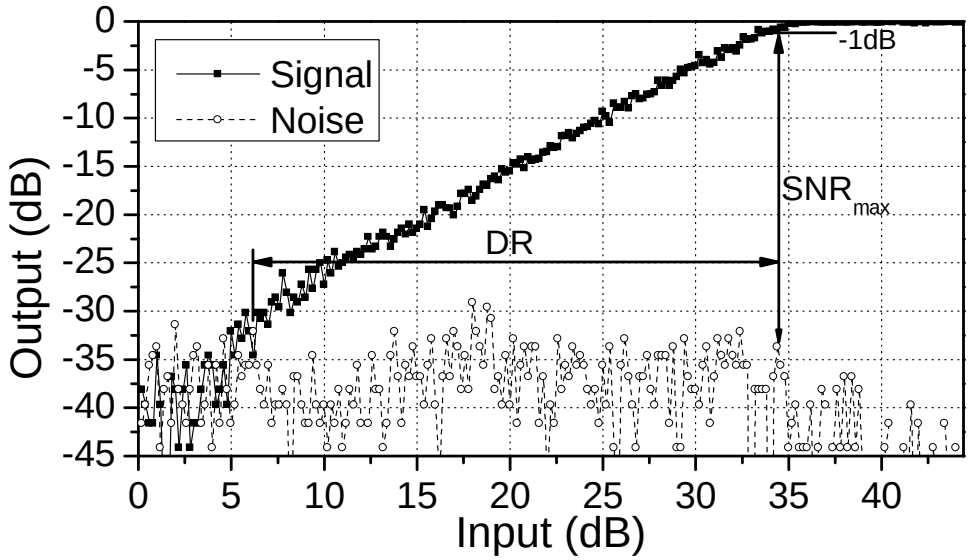
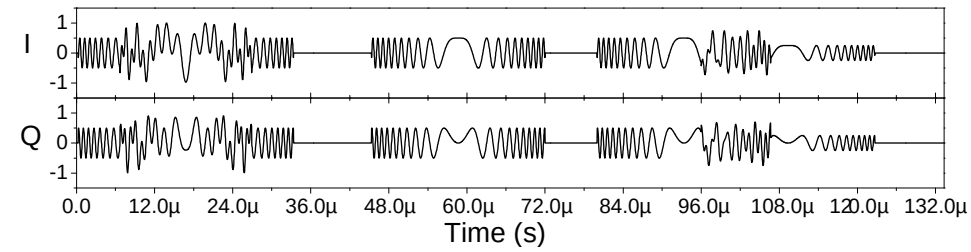


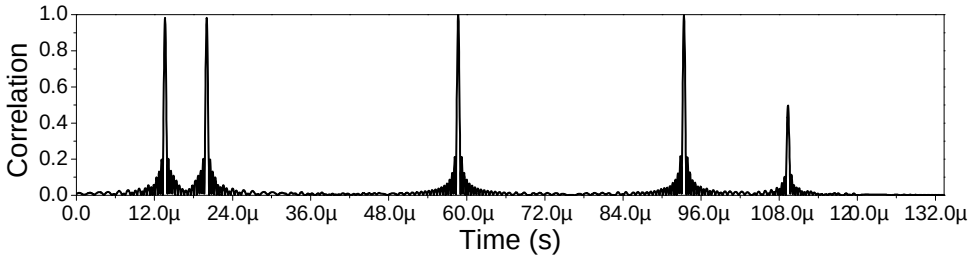
Figure 33: Measured output signal and noise characteristics with an input power sweep.

The maximum SNR measured as a difference between the output P_{1dB} to the output noise at the input P_{1dB} is 32.69 dB, and the DR from the input P_{1dB} point to the last point where SNR > 0 dB is 28.20 dB. Obviously, these values are much higher than the system level SNR and DR measured by using a chirp or a NLFM signal. In other words, the performance of the correlator seems not to be the limiting factor of the system.

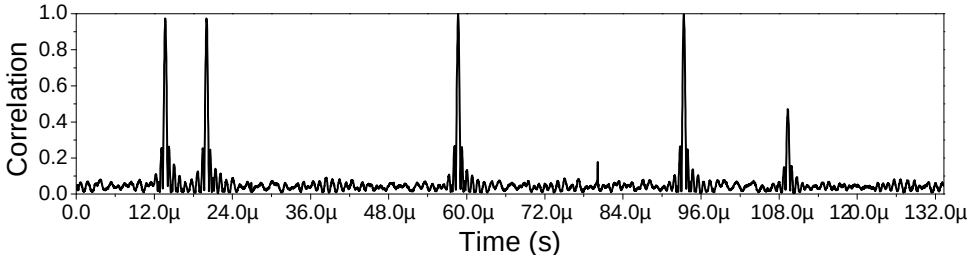
A measured pulse compressor response with that of a simulation in which multiple returns from targets are assumed to be present are compared in Figure 34.



(a)



(b)



(c)

Figure 34: (a) Input signals I and Q, (b) a simulated matched filter response, and (c) a measured matched filter response (average of 10) of multiple chirp signals.

Five overlapping chirp signal returns with bandwidth of 1.3 MHz and T of 26.7 μs centered at 13.39 μs, 20 μs, 58.65 μs, 93.33 μs, and 109.32 μs are added with relative amplitudes of 1/2, 1/2, 1/2, 1/2, and 1/4, and injected into the APC, which is triggered at the same time as the signal starts. Figure 34(a) shows that the first two and last two chirp signals overlap. Figure 34(b) shows the simulation results, and Figure 34(c) shows the experimentally obtained results by incrementing k by 1 each time. The sampled data were normalized to the maximum sampled value. The comparison between the simulated and measured compression results clearly shows

five distinctive pulses at corresponding times. The small peak at 80.13 μs may have come from the integrator dead time during the reset interval.

3.7 Conclusions

This research proposed a fully-integrated APC in a mixed signal domain using an analog correlator and an AWG to relax the requirements of speed and power for the ADC and the DSP. The APC was validated with results from various measurements using chirp signals and a wavelet. The detailed block specifications and the structures of the AWG, the analog correlator, and the ADC are explained. The system evaluation are performed using the proposed SNR and DR equations. The results of the evaluation showed that the proposed APC consumes about 62.6 mW when it is fully functional with a 1.8 V supply voltage, and the average SNR measured are 8.26 dB and 18.09 dB when a 1024-point chirp signal and a 1024-point NLFM signal were used. The SNR and the DR of the correlator were measured separately, and the system timing and functionalities were verified using multiple chirp signals. Table 2 summarizes the power consumption and the performance of the APC.

Table 2: Power and performance summary of the APC.

Process Technology			CMOS 0.18 μm
Core Size			$3.13 \times 1.81\,\mathrm{mm}^2$
Power	AWG	RAM	9.5 mW
		DAC	7.9 mW
		LPF	12.6 mW
	Analog correlator (total 2)	Integrator	11.9 mW
		Multiplier	7.9 mW
		Etc.	2.4 mW
	ADC (total 2) ($f_{CLK,ADC}$=1.2 MS/s)		7.9 mW
	Etc.		2.5 mW
	Total		62.6 mW
SNR	1024 point chirp		8.26 dB
	1024 point NLFM		18.09 dB
	Correlator		32.69 dB
DR	1024 point chirp		12.08 dB
	1024 point NLFM		20.54 dB
	Correlator		28.20 dB

CHAPTER IV

ENHANCED INPUT RANGE DYNAMIC COMPARATOR FOR PIPELINE ANALOG-TO-DIGITAL CONVERTER (ADC)

A new dynamic comparator with an enhanced input range is investigated in this chapter. Input trip point deviations from ideal values are shown to be less than those of a conventional comparator over a wide input range. This new dynamic comparator could be beneficial for low supply voltage ADCs, especially for low supply voltage pipeline ADCs.

4.1 Introduction

Switched-capacitor circuits are most commonly adopted for pipeline ADCs because the capacitor ratio is considered the most accurate component parameter in CMOS technology. Thus, a SC circuit can provide an accurate amplification factor, which is important for a high resolution ADC. Moreover, SC circuits can easily implement the sample-and-hold (S/H) block required for an ADC. In SC circuits, one of the most important decision factors for the minimum capacitor size is the kT/C noise, because this kT/C noise must be smaller than the least significant bit (LSB). In other words, $kT/C < V_{LSB,RMS}^2$ has to be satisfied, so that the kT/C noise does not degrade the performance of an ADC. Customarily, a value of kT/C is chosen that is at most half the value of $V_{LSB,RMS}^2$, because sufficient margins are required for other noise sources such as op-amp noise and switch noise. Because $V_{LSB,RMS}^2 = V_{FS}^2/(2 \times 2^n)$, where n is the resolution of an ADC and V_{FS} is the full-scale voltage of an input, $kT/C < V_{FS}^2/2^{n+1}$, and $C > kT2^{n+1}/V_{FS}^2$. Therefore, the size of a capacitor is

inversely proportional to the square of an input signal. Thus, a large signal voltage range will help to reduce the size of the capacitor, which will in turn help to reduce the size and power consumption of an ADC. However, with fabrication technology downscaling for low power and high speed, the supply voltage continues to shrink. Therefore, maximizing the input range within a given supply voltage becomes more important.

A comparator is one of the fundamental building blocks in analog circuits [40], and a dynamic comparator is commonly used in pipeline ADCs because it does not consume any static current, and its comparison time is short owing to strong regeneration from positive feedback [41–43]. Because a comparator in a pipeline ADC will experience the entire input range directly, maximizing the input range of a dynamic comparator is beneficial for a pipeline ADC.

4.2 Prior Arts

Many approaches have been proposed to increase the input range of a dynamic comparator. The most common approach has been to incorporate additional complementary amplifiers at the front end [44,45]. An op amp that simultaneously incorporates a p-type metaloxidesemiconductor (PMOS) input stage and an n-type metaloxidesemiconductor (NMOS) input stage can have its input range extended to entire rails by adding the transconductance (g_m) of a PMOS stage to that of an NMOS stage [46]. A PMOS input stage can have its input range from ground rail (V_{GND}) to $V_{DD} - V_{od,currentsource} - V_{thp}$, where V_{DD} is the supply voltage, $V_{od,currentsource}$ is the overdrive voltage of the current source, and V_{thp} is the threshold voltage of a PMOS transistor. An NMOS input stage can have its input range from $V_{GND} + V_{od,currentsource} + V_{thn}$, where V_{thn} is the threshold voltage of an NMOS transistor. In a modern CMOS process, $V_{od,currentsource}$ can be as low as around 100 mV, and V_{thp} and V_{thn} can each be around 200 mV. Therefore, by adding the g_m values of two complementary input

stages, this technique can produce a valid g_m over an entire input range. Even though g_m is not linear over the input range, this nonlinearity is usually not an important issue for an op amp because most op amps are used in a feedback configuration. Thus, the input range nonlinearity is linearized by feedback. For a comparator case, a complementary input preamp can be combined with a comparator to implement a wide input range comparator. However, this approach has higher power consumption because of the additional front-end stage.

An internally boosted supply voltage could be used [47]. In CMOS technology, MOS transistors can be used to implement switches without a voltage drop or bias current. Thus, it is viable to implement a capacitive charge boosting circuit internally, and to use the boosted voltage for an extended input range comparator. However, the complexity of the comparator will increase because of the boosting circuit, and significant noise can be generated from the boosting circuit because switches have to turn on and off quickly at every clock cycle.

Additional switches and capacitors could be utilized to implement a charge redistribution approach [43]. Because capacitors are passive devices, they can be connected to arbitrary voltages for charging, and can then be reconnected to desired voltages for charge redistribution. This approach is commonly used, but requires reference capacitors to be fully charged at every clock cycle and to be redistributed. Thus, the total power consumption will increase on top of the added circuit complexity.

In this chapter, an enhanced input range dynamic comparator is proposed and analyzed. This comparator overcomes the problems of the approaches listed above, while achieving a rail-to-rail input range. Therefore, a low voltage ADC design can benefit from this new dynamic comparator.

4.3 Conventional dynamic comparator

A conventional dynamic comparator is shown in Figure 35 [41].

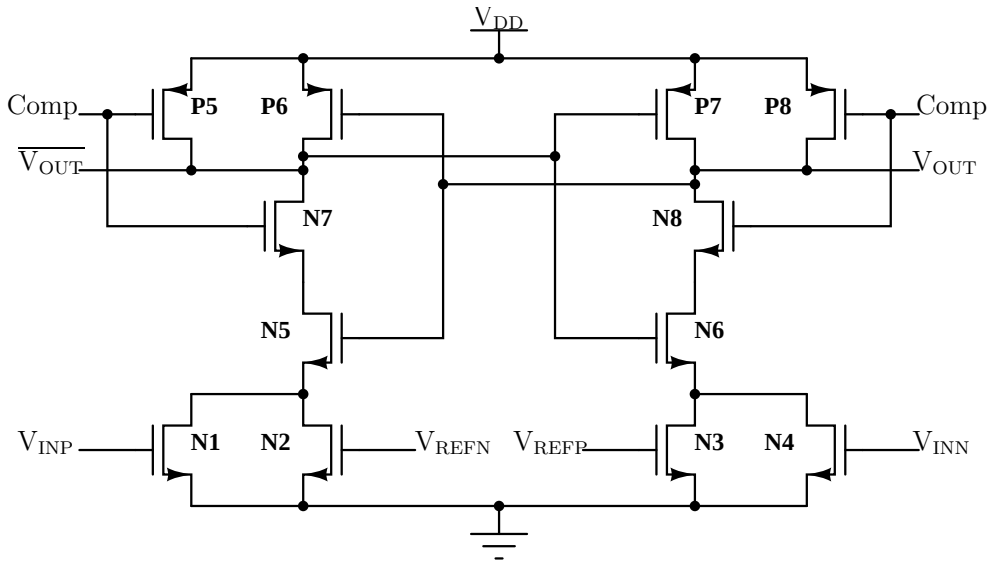


Figure 35: Conventional dynamic comparator.

If the comparison signal (Comp) starts low, the drains of transistors P5, P6, P7, and P8 are pre-charged to V_{DD}. Because transistors N7 and N8 are disconnected, the sources of transistors N5 and N6 will be at ground potential. A cross-coupled latch formed by P6, P7, N5, and N6 starts to regenerate when the comparison signal goes high. Transistors N1, N2, N3, and N4 start in a triode region because the sources of transistors N5 and N6 are discharged at this moment. The final state of the comparator is determined by the differences in the active resistances among N1, N2, N3, and N4 at the beginning of a comparison [41]. After some time, because the cross-coupled latch regenerates, either the drain voltages of N1 and N2 or those of N3 and N4 are pulled to V_{DD}, while the others remain at ground potential. Without a lack of generality, the drain voltages of transistors N1 and N2 can be assumed to be pulled to V_{DD}, while the drain voltages of transistors N3 and N4 can be assumed to remain at ground potential. Then, transistors N1 and N2 are no longer in a triode region. However, because of strong positive feedback, the drain voltages of transistors N1 and N2 have to keep increasing, while the drain voltages of N3 and N4 remain at ground potential regardless of the voltages applied at the gate nodes of the transistors.

In other words, the gate voltages of N1, N2, N3, and N4 can no longer affect the final value of the comparator, but only the initial gate voltages are important. After the drain voltages of N1 and N2 reach their final value of V_{DD} and the drain voltages of N3 and N4 reach their final value of ground potential, transistors N5 and P7 go into a cut-off region. Thus, both the left and right current paths are blocked, and there is no more current flow in either of the branches. This comparator is called a "dynamic comparator" because of this property, and its internal nodes have to be reset at every comparison cycle. However, owing to the strong positive feedback, the comparison is fast, and the power consumption is zero after the outputs are resolved.

If the widths of N1, N2, N3, and N4 are chosen to be $kW_{N1} = kW_{N4} = W_{N2} = W_{N3}$ with a certain constant, k, and they have the same channel lengths, L, then the trip point of this comparator to the first order with respect to a differential input voltage, $V_{IN} = V_{INP} - V_{INN}$, and a differential reference voltage, $V_{REF} = V_{REFP} - V_{REFN}$, is given as follows [41].

$$V_{IN,trippoint} = kV_{REF} \tag{14}$$

However, the above equation is derived assuming that all of the transistors, N1, N2, N3, and N4, are in a strong inversion region. If any of the $V_{INP}, V_{INN}, V_{REFP}, V_{REFN}$ are below the NMOS threshold voltage (V_{thn}), then that particular transistor is not in a strong inversion region, and the above equation is no longer valid. Therefore, the input and reference signals should be higher than V_{thn} for this comparator to operate as expected. This greatly restricts the input and reference voltage ranges of a comparator because in modern CMOS technology, the supply voltage is quite often less than 1 V, while the threshold voltage (V_{thn}) could be more than 200 mV. This problem is even worse at a more advanced technology node because the supply voltage continues to scale down, while the threshold voltage remains more or less the same.

A pipeline ADC with redundancy and digital correction is somewhat tolerant of

a comparator offset [41]. For example, a commonly used 1.5 b/stage pipeline ADC is tolerant of a comparator offset as large as $V_{REF}/4$. However, even in this case, the overall offset margin will be reduced because of the above mentioned restriction. If the supply voltage and reference voltage are 1.8 V, then $V_{REF}/4$ is 450 mV. If the threshold voltage is 200 mV, then 44% of a margin is already consumed by this restriction. Therefore, even for a pipeline ADC with redundancy, a comparator with a wide input range is beneficial.

4.4 Complementary input dynamic comparator (CIDC)

Figure 36 shows a new complementary input dynamic comparator (CIDC).

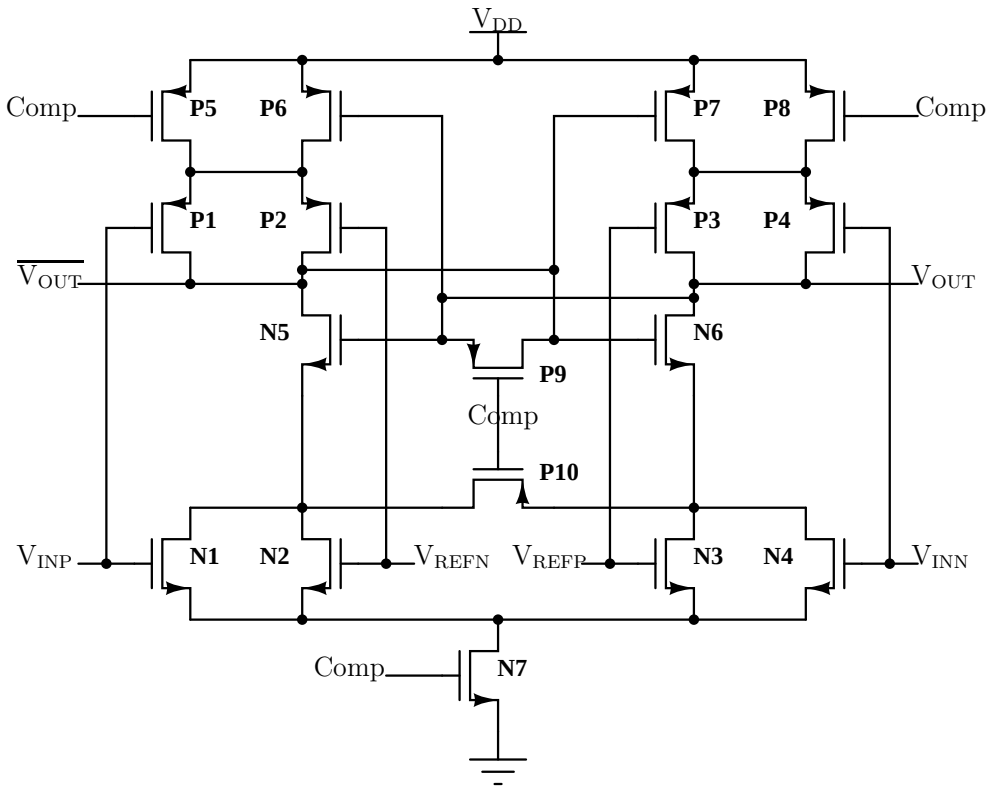


Figure 36: Complementary input dynamic comparator (CIDC).

When the comparison signal (Comp) is low, the comparator is in the reset mode. Similar to the conventional comparator case, the drain voltages of the PMOS transistors, P1, P2, P3, P4, P5, P6, P7, and P8, are pre-charged to V_{DD}. Transistors P9

and P10 function as equalizers, which help to balance mismatches among the drain voltages of transistor P1, P2, P3, and P4, and N1, N2, N3, and N4, respectively. Because the drains of transistors N5 and N6 are pre-charged to V_{DD}, and the drains of N2 and N3 are also pre-charged to V_{DD} through transistors N5 and N6, transistors P9 and P10 do not seem to be necessary at a first glance. However, there can be mismatches between reset transistors P5 and P8, and between transistors N5 and N6, which P9 and P10 help to overcome.

When signal Comp goes high, a cross-coupled inverter pair formed by transistors N5, N6, P6, and P7 starts to regenerate. Let us first assume that complementary transistors P1, P2, P3, and P4 and N1, N2, N3, and N4 start in a triode region. With the same transistor channel lengths, L, the active resistances, R_{N12} of the N1, N2 pair and R_{N34} of the N3, N4 pair, are given to the first order by the following equations.

$$\frac{1}{R_{N12}} = \mu_n C_{ox}\left[\frac{W_{N1}}{L}(V_{INP} - V_{thn} - V_{D,N7}) + \frac{W_{N2}}{L}(V_{REFN} - V_{thn} - V_{D,N7})\right]$$

$$\frac{1}{R_{N34}} = \mu_n C_{ox}\left[\frac{W_{N4}}{L}(V_{INN} - V_{thn} - V_{D,N7}) + \frac{W_{N3}}{L}(V_{REFP} - V_{thn} - V_{D,N7})\right]$$

In the above equations, $V_{D,N7}$ is the drain voltage of N7. With the PMOS threshold voltage, V_{thp}, the active resistances, R_{P12} of the P1, P2 pair and R_{P34} of the P3, P4 pair, are given as follows.

$$\frac{1}{R_{P12}} = \mu_p C_{ox}\left[\frac{W_{P1}}{L}(V_{DD} - V_{INP} - |V_{thp}|) + \frac{W_{P2}}{L}(V_{DD} - V_{REFN} - |V_{thp}|)\right]$$

$$\frac{1}{R_{P34}} = \mu_p C_{ox}\left[\frac{W_{P4}}{L}(V_{DD} - V_{INN} - |V_{thp}|) + \frac{W_{P3}}{L}(V_{DD} - V_{REFP} - |V_{thp}|)\right]$$

Because the initial instantaneous currents at the drains of N5, and N6 are proportional to $1/R_{P12} - 1/R_{N12}$ and $1/R_{P34} - 1/R_{N34}$ respectively, the trip point of the comparator can be calculated from these two as follows.

$$\frac{1}{R_{P12}} + \frac{1}{R_{N34}} = \frac{1}{R_{N12}} + \frac{1}{R_{P34}} \tag{15}$$

If the transistor widths are set as $kW_{N1} = kW_{N4} = W_{N2} = W_{N3}$, $kW_{P1} = kW_{P4} = W_{P2} = W_{P3}$, and $\mu_n W_{N1} = \mu_p W_{P1}$, then by simple algebra, (15) can be simplified to $V_{INP} - V_{INN} = k(V_{REFP} - V_{REFN})$ from the $1/R_{N12}$, $1/R_{N34}$, $1/R_{P12}$, and $1/R_{P34}$ equations shown above. Thus, the CIDC trip point is the same as (14), which is the equation for a conventional comparator. Even though both the PMOS transistor and NMOS transistor are assumed to be in a triode region at the start of operation, if the input range is high, such that the PMOS transistors are not in a strong inversion region, then $1/R_{P12}, 1/R_{P34}$ in (15) become zero except for a negligible sub-threshold conductance. Therefore, the behavior of this comparator will be governed by the equation, $1/R_{N34} = 1/R_{N12}$, which is the same as a conventional comparator. When the input range is too low, such that the NMOS transistors are not in a strong inversion region, then (15) becomes $1/R_{P12} = 1/R_{P34}$, because $1/R_{N12}$ and $1/R_{N34}$ become negligible. In this case, the trip point is determined as follows.

$$\mu_p C_{ox}\left[\frac{W_{P1}}{L}(V_{DD} - V_{INP} - |V_{thp}|) + \frac{W_{P2}}{L}(V_{DD} - V_{REFN} - |V_{thp}|)\right]$$
$$= \mu_p C_{ox}\left[\frac{W_{P4}}{L}(V_{DD} - V_{INN} - |V_{thp}|) + \frac{W_{P3}}{L}(V_{DD} - V_{REFP} - |V_{thp}|)\right]$$

$$V_{INP} + kV_{REFN} = V_{INN} + kV_{REFP}$$

$$V_{INP} - V_{INN} = k(V_{REFP} - V_{REFN})$$

Therefore, the trip point is the same as (14) again.

In this section, by simple first-order calculations, CIDC was shown to have a wider range than that of a conventional comparator, while the trip point was determined by the same equation as a conventional comparator. Notice that a wide input range has been achieved without additional preamp stages, boosted supply voltage, or capacitors. Even though this scheme requires more transistors, the static power consumption is still zero, except for a negligible sub-threshold current. Moreover, the input voltages or reference voltages are still applied to the gates of the transistors directly, so no additional charging current is required.

4.5 Simulations

Both types of comparators were realized with the TSMC CMOS 0.18–μm process, and simulations were performed using a Cadence® Spectre® simulator. The transistors were sized to satisfy $k = 1/4$, which is a commonly used ratio for pipeline ADCs with a 1.5 b/stage architecture. For a fair comparison, the sizes of P5-P8 and N1-N7 were kept the same for the conventional comparator and new CIDC. To compare the trip point error difference between the cases, $V_{error,trippoint} = V_{IN,trippoint} - V_{REF}/4$ was calculated from the simulation results because the ideal trip point, $V_{IN,trippoint}$, is $V_{REF}/4$ according to (14) when $k = 1/4$. V_{REF} was fixed and V_{IN} was swept in 10-mV steps to find a trip point ($V_{IN,trippoint}$) by measuring output voltage V_{OUT} at 1.0 ns. A value of 1.0 ns was chosen because it was found by simulations that the outputs of both comparators reached at least 80% of their final states at 1.0 ns from a starting time of 0 second. Figure 37 shows the trip point errors at the two common mode voltages, $V_{CM} = (V_{INP} + V_{INN})/2 = (V_{REFP} + V_{REFN})/2$, of 0.9 V and 1.2 V.

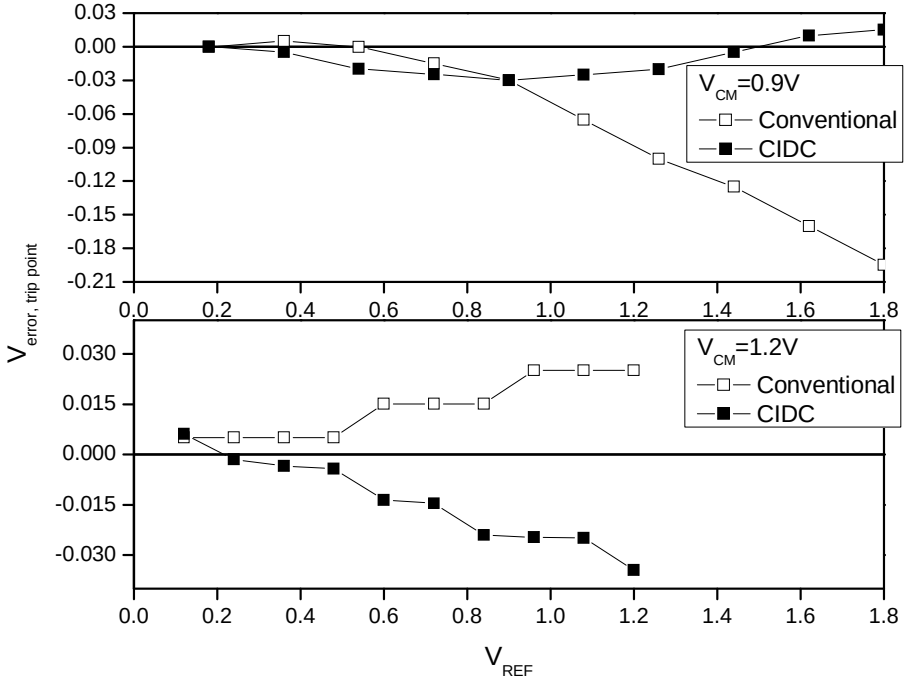


Figure 37: Trip point errors with V_{REF} and V_{CM} sweep.

It can be seen that when the common mode voltage was high ($V_{CM} = 1.2\,\mathrm{V}$), the maximum V_{REF} was 1.2 V from the limit of the 1.8 V supply voltage, because $(1.8 - 1.2) \times 2{=}1.2\,(\mathrm{V})$, and both approaches had comparable maximum errors of about 40 mV. However, when the common mode voltage was low ($V_{CM} = 0.9\,\mathrm{V}$), the maximum V_{REF} was 1.8 V, and the conventional comparator could have an error of more than 200 mV, while the errors of the CIDC stayed within 30 mV over the entire input voltage range. The voltage error for the conventional comparator became large because when V_{REFN} was lower than V_{thn}, equation (14) no longer holds. Even though the trip point could be re-calculated, assuming the transistor with the V_{REFN} voltage input at its gate was in a cut-off region, this new equation could only cover the narrow input range for a case where $V_{REFN} < V_{thn}$. Therefore, because the common mode voltage range of the CIDC could go lower, it was wider than that of the conventional

comparator.

Next, Monte Carlo simulations were performed considering mismatches between the transistors to compare the robustness of the comparators when there were mismatches. Figure 38 shows histograms of the results.

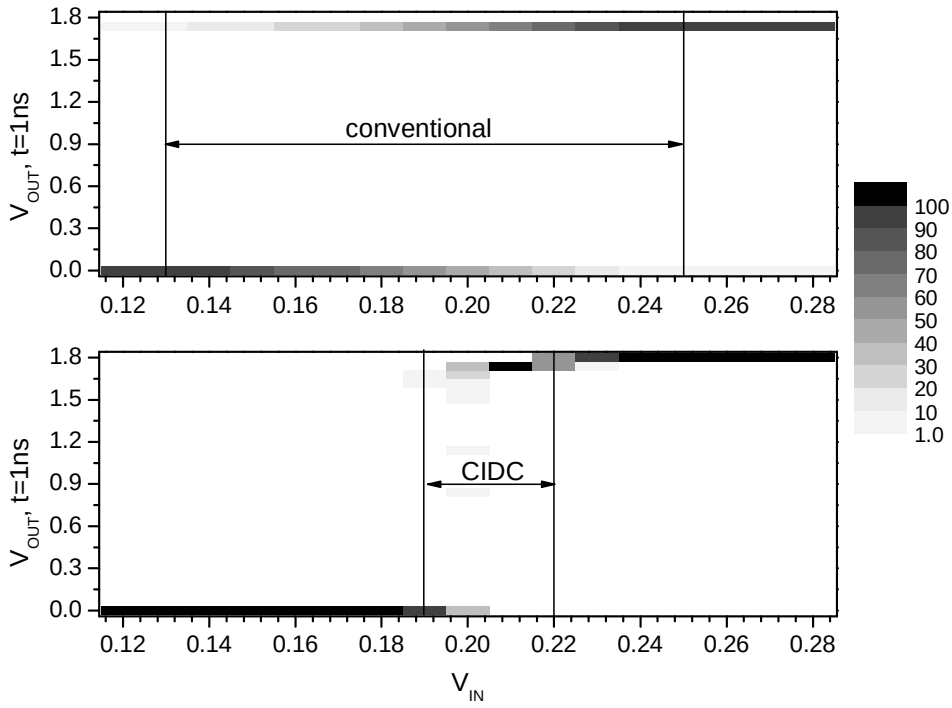


Figure 38: Histogram of Monte Carlo simulation.

For fair comparisons, $V_{CM} = V_{REF} = 0.9\,\mathrm{V}$ (ideal $V_{IN,trippoint} = 0.225\,\mathrm{V}$) was chosen as the simulation point because, from Figure 37, the trip point errors were found to be comparable, -30 mV, at these conditions. For each input voltage V_{IN}, 100 samples were simulated with random variations and were put into bins according to V_{OUT} at 1.0 ns. As shown in Figure 38, the spread of the input trip points with less than 95% (2σ) correct output was 120 mV for the conventional comparator and 30 mV for the CIDC. Even though the CIDC required more transistors than the

conventional comparator, these additional transistors could exacerbate the mismatch variation while reducing the trip point error. Therefore, the additional transistors did not degrade the mismatch performance. In addition, equalizing transistors P9, P10 contributed to mismatch immunity. However, it is worth noting that while the conventional comparator had clear transitions at 1.0 ns, the output of the CIDC may not have a clear transition at 1.0 ns, as shown by the gray boxes at the V_{OUT} of around 1.1 V. This metastability may have come from the fact that the CIDC had both NMOS and PMOS transistors connected together, which degraded the regeneration time constant. The regeneration time constant τ of a cross-coupled inverter can be approximated as $(g_{mp} + g_{mn})/(C_{gsp} + C_{gsn})$, where g_{mp} is the transconductance of a PMOS transistor, g_{mn} is the transconductance of an NMOS transistor, C_{gsp} is the gate capacitance of a PMOS transistor, and C_{gsn} is the gate capacitance of an NMOS transistor. Because the CIDC had larger series resistances caused by stacking the NMOS and PMOS transistors, g_{mp} and g_{mn} of the CIDC were at most half of the values in the conventional comparator. However, this weakness could be compensated for by using longer widths for transistors N1, N2, N3, N4, P1, P2, P3, and P4 at the cost of increased gate capacitance. With an increased transistor size, the gate driving circuit strength would also have to be increased to prevent a speed penalty. In other words, there is a trade-off for a CIDC among the input driving circuit strength, input transistor size, and speed. In a conventional comparator case, longer widths for transistors N1, N2, N3, and N4 alone do not help to increase the input range. Thus, a trade-off such as described for a CIDC is not possible.

4.6 Conclusion

An enhanced input range dynamic comparator was proposed, and its input range was compared with that of a conventional dynamic comparator using calculations and simulations. First order calculations showed that the CIDC had an enhanced

input range while keeping the same trip point as a conventional comparator without additional stages or higher power consumption. Simulations verified that the CIDC had less trip point error than a conventional comparator. Monte Carlo simulation results indicated that the CIDC was robust to device mismatches with only a minor speed penalty. With these advantages, the use of a CIDC could help to reduce the size and power consumption of an ADC.

CHAPTER V

ANALOG-TO-DIGITAL CONVERTER (ADC) BASED ON THE ASYNCHRONOUS SUCCESSIVE APPROXIMATION REGISTER (SAR)

An ADC is required at the end of mixed-signal processing to convert analog signals to digital signals for further digital signal processing. However, an ADC occupies a significant portion of a system budget for the power consumption, so improvement of an ADC will greatly enhance various trade-offs. Also, fundamental trade-offs/limits among signal, noise, bandwidth, and power for an ADC is currently an active area of research.

In this chapter, a new architecture of a low-power ADC based on an asynchronous sample-and-hold multiplying SAR (ASHMSAR) for MIMO applications will be investigated. Furthermore, detailed design and implementation issues for an ADC in CMOS technology will be discussed. MIMO applications could benefit from the lower power consumption of a new ADC without system performance degradation.

5.1 Trends

Since the invention of the ADC, many different architectures have been proposed. However, one single architecture cannot cover the entire spectrum of the applications, and a particular architecture is chosen mainly according to the sampling frequency and ENOB requirements of the system of interest. Figure 39 [10] shows the distribution of ADC architectures according to their ENOB and the sampling rate, and clearly illustrates that some architectures dominate at certain regions of the graph.

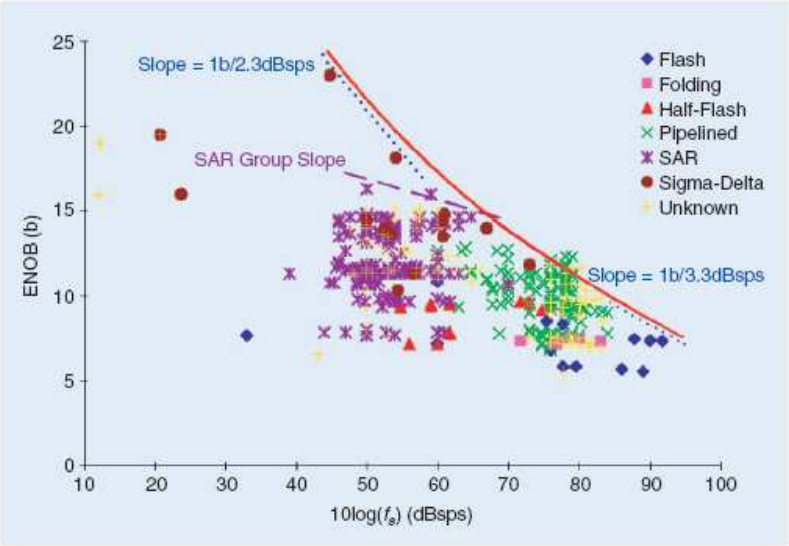


Figure 39: ENOB versus sampling rate [10].

For a wireless system, the most commonly required sampling rate falls around ten megahertz with around ten ENOB, so a pipeline architecture is most often chosen for these applications.

Figure 40 presents a survey on the current state of the art ADCs published in two major conferences, International Solid-State Circuits Conference (ISSCC) and VLSI Technology Symposium (VLSI) with Walden FOM, $\frac{P}{2 \cdot BW \cdot 2^{ENOB}}$, as the x coordinate, and the ADC performance index, $2 \cdot BW \cdot 2^{ENOB}$, as the y coordinate.

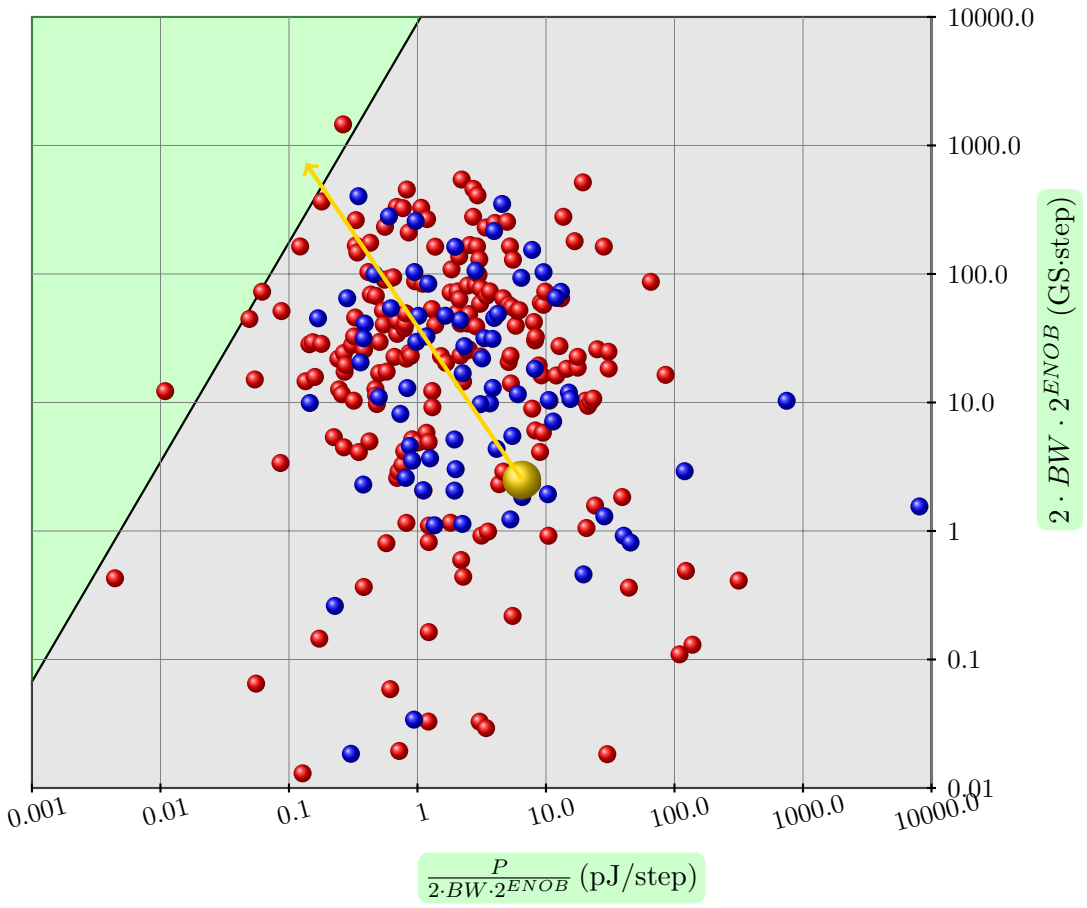


Figure 40: Survey of the published ADC performances from ISSCC (red) and VLSI (blue) of year 1997–2009 [48].

Since a small value for an x-coordinate and a large value for a y-coordinate is desirable, a line could be drawn at the left upper corner by the linear least squares fitting techniques on nearby data points. The line and the area divided by this line is shown in Figure 40.

The ADC presented in Subsection 3.5.3 is shown as a yellow ball in the above figure, which is moving toward the area in the upper left corner as indicated by an arrow. This ADC is highly desirable. If a new ADC can achieve the sampling rate of 80–100 MS/s, ENOB of 12–14 b, and power consumption of 54–72 mW, the improvement of FOM will be ×1/30, BW ×4.2, SNR +30 dB, an ADC performance index of ×4.4, indicating that the APC performance can be increased dramatically

with a new ADC without a significant penalty on power consumption.

Recently, many new ideas have been published to overcome previous limitations. One of the most common solutions is to replace the power consuming op amp with another block or not to use the op amp at all. The efficiency of a class-A op amp in a SC circuit is inversely proportional to the number of τ, the time constant. For example, if the settling time t_{settle} is longer than 10 times of τ, (i.e. $t_{settle} > 10\tau$), the charge delivered to the load is only a few percent of the charge drawn from the supply [11]. Since τ has to be larger than approximately $N \ln 2$ for N-bit accuracy, the efficiency of an op amp is troublesome, especially for an ADC with high accuracy.

For example, an ADC based on an asynchronous binary search [27] as in Figure 41 is based purely on a comparator without using a power-inefficient op amp.

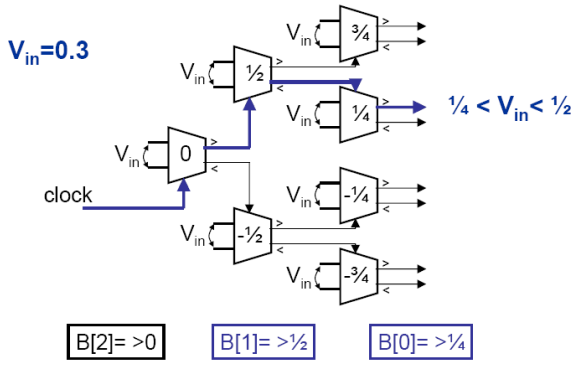
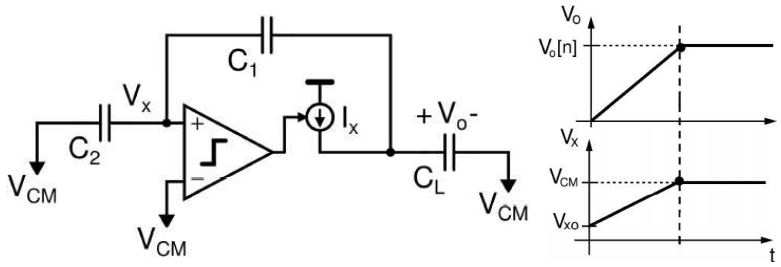


Figure 41: Implementation of a binary search with comparators (3 bits shown) [27].

Since this architecture searches the predetermined binary tree according to the current comparison results, the settling issue with a conventional SAR does not exist, so comparisons can be fast. Moreover, the branch which is not used can be powered off to reduce power consumption even further.

An ADC based on a zero-crossing detector [25] as in Figure 42 is also based on the idea of not using op amps. A comparator alone is utilized to form an amplifier in a feedback form without an op amp.



(a) (b)

Figure 42: Illustration of (a) the zero-crossing based circuit, and (b) voltage waveforms [25].

Since this architecture is based on comparators only, many basic circuit techniques, such as common-mode feedback, are not applicable to this ADC, so all these detailed techniques have to be developed again. Also, ENOB higher than 11 could pose difficulties because of the accuracy of the turn-off point and charge injection. This circuit could be more sensitive to clock jitter than a conventional pipeline architecture as well.

An ADC based on the capacitive charge pump (CP) [49] in Figure 43 is another architecture to remove op amps.

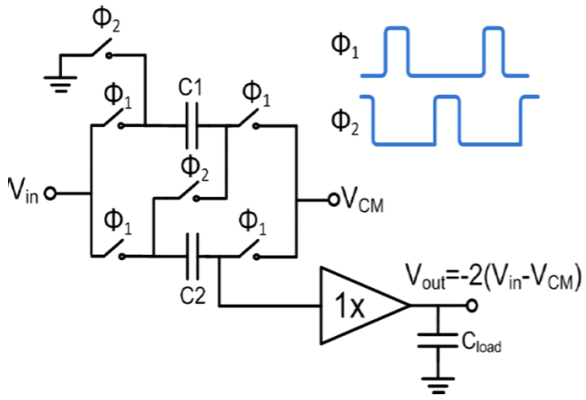


Figure 43: 2x gain using a charge pump [49].

After charged parallel, capacitors can be reconfigured in series to increase the voltage such that the input voltage will be multiplied. However, accuracy could be

limited because of charge injection or other leakage issues, so calibration is necessary [49].

A multi-bit front-end, SHA-less architecture is also popular. Figure 44 illustrates one implementation.

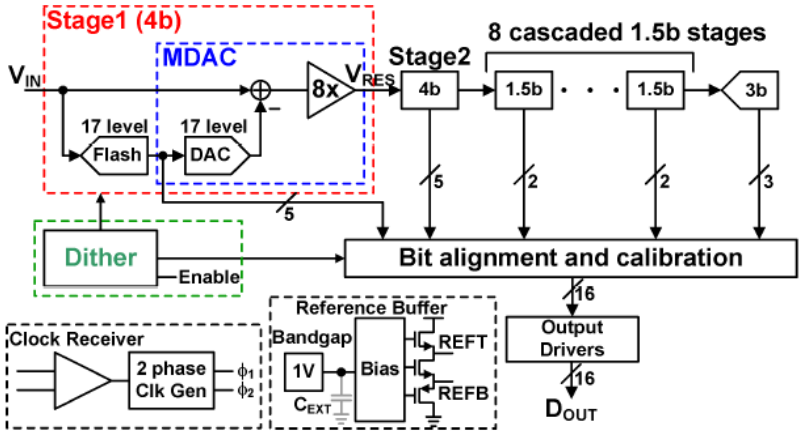


Figure 44: Pipeline ADC architecture [50].

A sample-and-hold amplifier at the front end of an ADC does not contribute to bits resolution, but it consumes the highest power among blocks of the pipeline chain. Therefore, if sampling could be performed accurately without an amplifier, then the total power consumption could be reduced dramatically. Also, resolving multi bits at the first stage, which is highly desirable, will be explained in detail in Section 5.2.

5.2 Background

A typical pipeline ADC architecture [41, 42, 51, 52] is shown in Figure 45, assuming one extra bit for the digital correction.

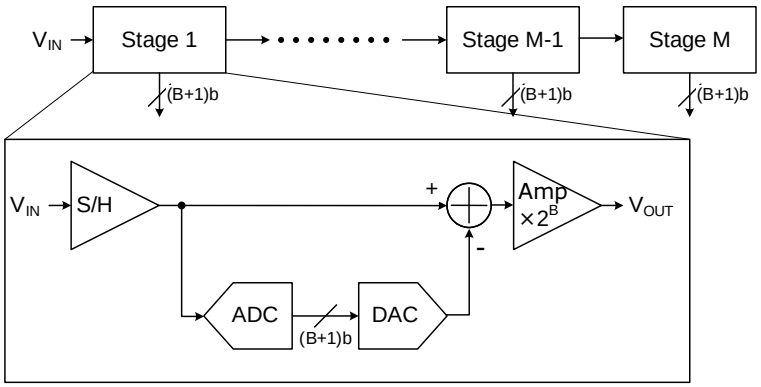


Figure 45: Typical pipeline architecture [51].

Each stage samples the signal from the previous stage and quantizes it in 2^{B+1} resolution with a sub-ADC, which is commonly implemented by a flash architecture. Then, the quantized value is converted to an analog value by a DAC and then subtracted from the input signal. This residue is multiplied by 2^B, and the amplified signal is fed into the next stage. This step is repeated through all stages.

One of the key design parameters is B, the gain per stage. Since each stage requires 2^{B+1} comparators in the sub-ADC, reducing B will reduce the total number of comparators. However, by resolving B bits at each stage, the requirements for subsequent stages are relaxed, as illustrated in Figure 46.

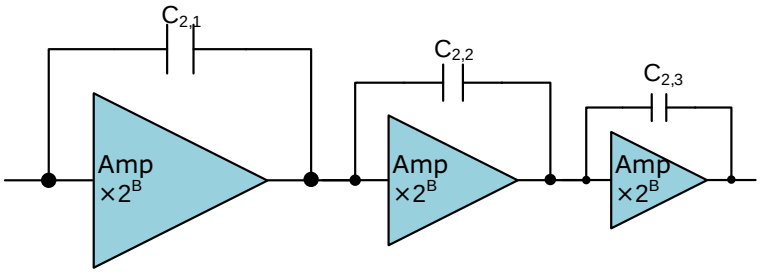


Figure 46: Scaling of each stage in a pipeline ADC.

The amplifier in Figure 45 is commonly implemented using a SC op-amp circuit as in Figure 47. For clarity of explanation, only half of the differential circuit is shown.

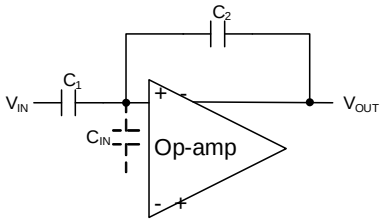


Figure 47: Typical SC amplifier.

Let's assume the open-loop gain of the op amp at the first stage is $A_{0,0}$. Then, the feedback factor f is

$$f = \frac{C_2}{C_1 + C_2 + C_{IN}},$$

and with the capacitor turn-around scheme being the multiply-by-two scheme [53], the transfer function is

$$\frac{V_{OUT}}{V_{IN}} = \frac{C_1 + C_2}{C_2} = 2^B,$$

with an approximate gain error [46] of

$$\frac{C_1 + C_2 + C_{IN}}{A_{0,0} C_2}.$$

Therefore, if the total ADC resolution target is N, $A_{0,0}$ must satisfy

$$\begin{aligned} 2^{-(N-B)} &> \frac{C_1 + C_2 + C_{IN}}{A_{0,0} C_2} \\ A_{0,0} &> 2^{N-B} \frac{C_1 + C_2 + C_{IN}}{C_2} \\ A_{0,0} &> 2^{N-B} \left(2^B + \frac{C_{IN}}{C_2} \right) \\ A_{0,0} &> 2^N \left(1 + \frac{C_{IN}}{2^B C_2} \right). \end{aligned}$$

The open-loop gain $A_{0,1}$ of the second stage must satisfy

$$\begin{aligned} 2^{-(N-2B)} &> \frac{C_1 + C_2 + C_{IN}}{A_{0,1} C_2} \\ A_{0,1} &> 2^{N-2B} \left(2^B + \frac{C_{IN}}{C_2} \right) \\ A_{0,1} &> 2^{N-B} \left(1 + \frac{C_{IN}}{2^B C_2} \right). \end{aligned}$$

In general, the k-th stage open loop gain $A_{0,k-1}$ must satisfy

$$A_{0,k-1} > 2^{N-kB}\left(1+\frac{C_{IN}}{2^B C_2}\right). \tag{16}$$

In practice, there could be many different factors to consider. For example, if $C_{2,k}$ is scaled as $\frac{C_{2,1}}{2^{2kB}}$, then the noise contribution for each stage is equal [52]. However, the above simplified analysis shows that the requirements for each stage lessen as k increases, and this reduction in requirements in turn results in a power savings, which also implies that the requirements for the first stage are the most stringent. This is especially the case if it is required to have a separate sample-and-hold (S/H) stage since the requirements for the S/H will be the most stringent without reducing requirements for the subsequent stages. This is why merging S/H with the first multiplying DAC (MDAC) is currently being actively investigated by many researchers [54].

5.3 Design Approach

5.3.1 Pipeline utilizing SAR

From (16), it can be seen that the requirements for subsequent stages can be relaxed more steeply by having high resolution per stage ($B > 3$) while saving power because of the smaller number of op amps. However, implementing a sub-ADC with a flash-type architecture for more than 3 bits is problematic since the required number of comparators per stage increases exponentially with B as 2^{B+1}. Therefore, different sub-ADC architectures that allow high resolution without exponential complexity such as a folding and interpolation ADC with $B = 6$ for the first stage [55] has been actively investigated. An asynchronous SAR ADC that can provide higher than 3-bit resolution with linear complexity [56], is a power efficient architecture. However, it is difficult to obtain high resolution, high speed, and small die area at the same time with the SAR architecture alone. Therefore, a pipeline ADC with an asynchronous sample-and-hold multiplying SAR (ASHMSAR) that merges a S/H, a capacitor DAC (CDAC), a comparator, and latches all together is proposed. The

pipeline architecture can benefit from the ASHMSAR due to high $B > 3$ without exponential complexity, and the integration of ASHMSAR into the pipeline architecture can provide high resolution. Also, since a separate power consuming S/H is not required, further power saving is obtained. Further, the proposed ASHMSAR includes a scheme that needs only one comparator for three-level (1.5 bit) comparison by exploiting the metastability inherent in a comparator. The proposed architecture may be able to provide a improved trade-off among power, resolution, speed, and die area.

5.3.2 Metastability

A commonly used latch-type comparator can be approximately modeled as in Figure 48(a) [57]. Therefore, the output $V_X - V_Y$ is evaluated as the following equation.

$$V_X - V_Y = V_{XY0} e^{(A_0 - 1)\frac{t}{\tau_0}}$$

A typical waveform is depicted in Figure 48(b). If the input to the comparator is very close to the comparison point, the output settling time can be infinite. In other words, if $V_{XY0} \to 0$, then $t|_{V_X(t) - V_Y(t) > V_{XY1}} \to \infty$ (See Figure 48(c)). This phenomenon is commonly referred to as metastability.

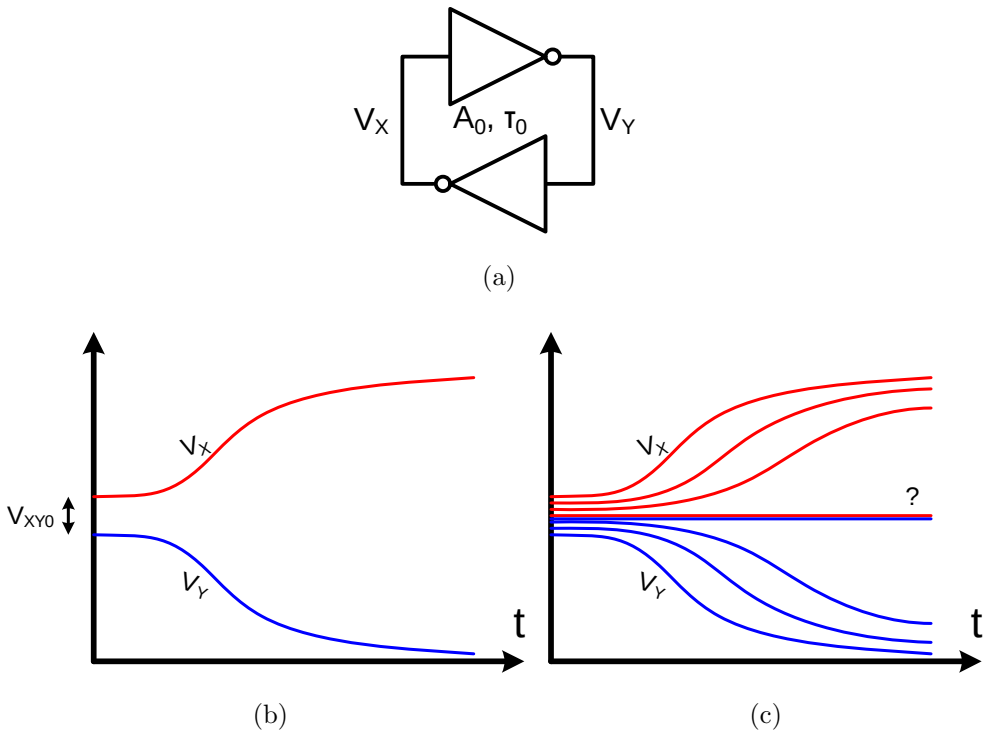
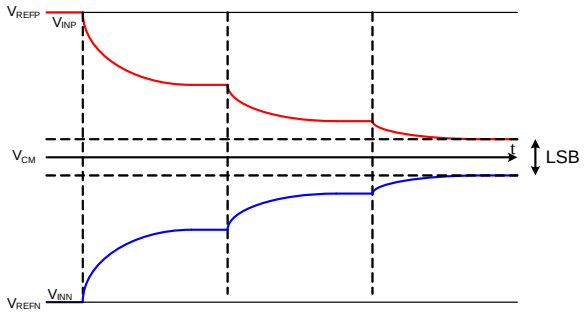


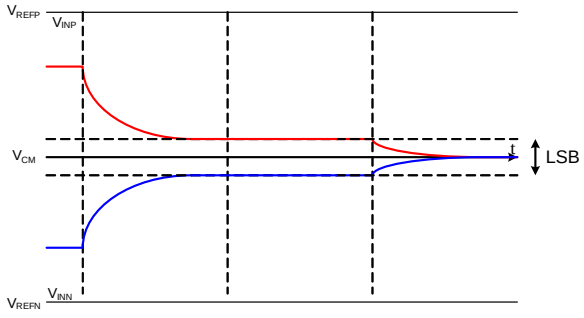
Figure 48: Metastability of a latch-type comparator.

Therefore, if metastability state is regarded as another state, each stage can generate three levels (1.5 bit) with only one comparator. However, this scheme is problematic when the input is just high enough that the most significant bit (MSB) trips at the end of SAR cycle. Then, the residue can be much higher than desired one LSB. To overcome this problem, a 'skipping scheme' has been implemented instead of a infinite wait scheme as above while still providing three level (1.5 bit) comparison with only one comparator exploiting metastability. This idea is explained in detail in following paragraphs.

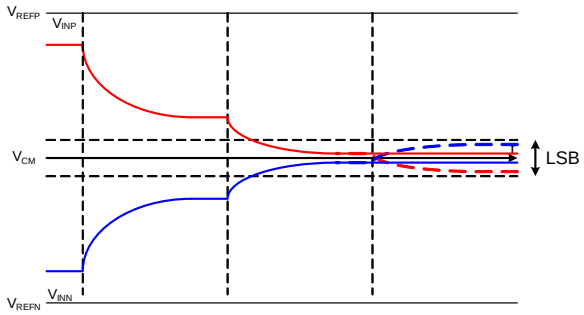
The purpose of a SAR is to make the residue less than one LSB by subtracting or adding scaled reference voltages at each step as in Figure 49(a). However, if any approximation step is allowed to be skipped when the residue is smaller than a certain value, this scheme is likely to generate smaller residue than the conventional scheme (See Figure 49(b)–(c)).



(a)



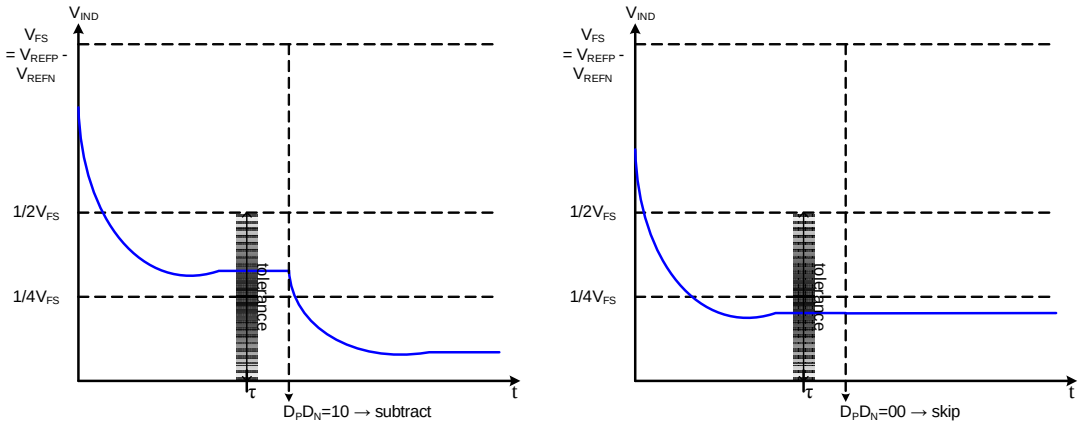
(b)



(c)

Figure 49: SAR operation of (a) a typical case, (b) a case with a small 2nd residue, and (c) a case which has smaller residue without subtraction.

This idea can be further explained by Figure 50. If the signal is over the threshold with a given time τ, the signal will be subtracted, as in Figure 50(a). The timing will be further explained in Subsection 5.4.2. However, if the signal is under the threshold with a given time τ, the successive approximation operation will skip to the next stage without DAC subtraction/addition (Figure 50(b)).



(a) (b)

Figure 50: When the signal is (a) above the threshold, and (b) below the threshold with a given time τ.

Therefore, if the metastability state is considered as another state, only one comparator can generate a total of three states as following equations.

$$\begin{cases} D_P D_N = 00 \\ D_P D_N = 10 \\ D_P D_N = 01 \end{cases}$$

The residue plot of this scheme is compared with that of the conventional scheme in Figure 51.

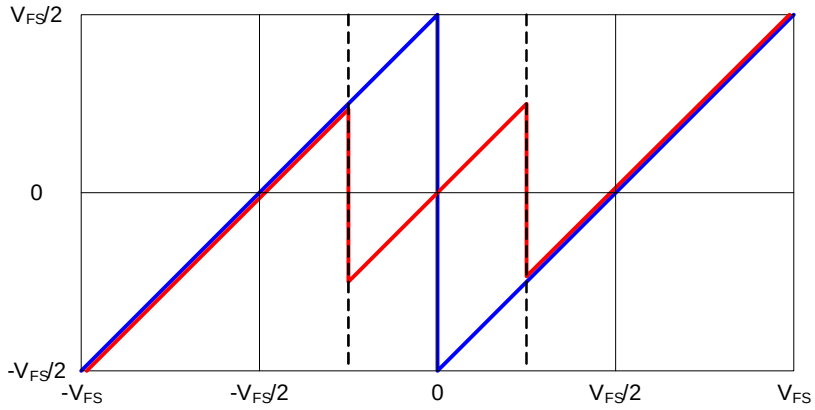


Figure 51: Residue plot of the conventional scheme (blue), and the proposed scheme (red).

Since the 1.5 b/stage scheme can tolerate a maximum $V_{FS}/4$ offset [41], τ can have significant margins. Figure 52 shows the residue plot for three different cases when $\tau = \tau_{nom}$, $\tau < \tau_{nom}$, and $\tau > \tau_{nom}$, where τ_{nom} is the nominal value.

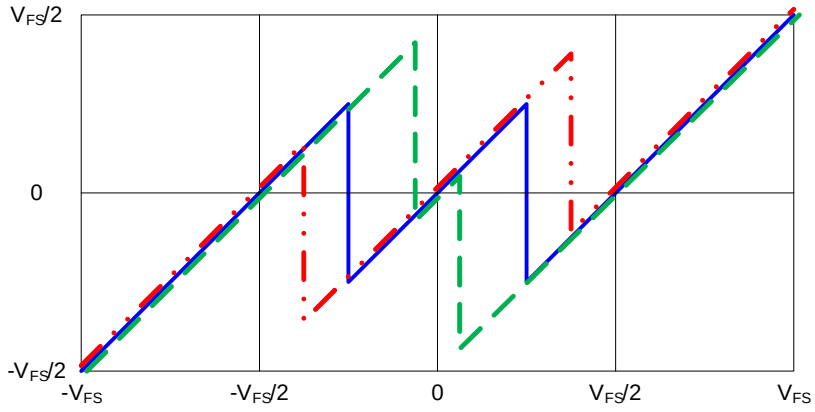


Figure 52: First stage residue plot of ASHMSAR when $\tau = \tau_{nom}$ (solid line), $\tau > \tau_{nom}$ (dotted line), and $\tau < \tau_{nom}$ (double dotted line).

When $\tau = \tau_{nom}$, the comparison will occur exactly at the $\pm V_{FS}/4$. However, when $\tau < \tau_{nom}$, the comparison levels will shift outward since the signals do not have enough time to fully settle. If τ is set to too small, there is a danger that the comparison levels may go beyond $\pm V_{FS}/2$. Therefore, a minimum τ is required and

will be calculated in Subsection 5.4.4.

On the other hand, when $\tau > \tau_{nom}$, the comparison levels will shift inward since the signals has too much time to be amplified by the preamplifier such that the center zone in the middle will shrink. However, this center zone cannot shrink to zero because theoretically the metastability requires $\tau = \infty$ to have a zero center zone. In other words, the center zone always exists regardless of τ.

In all cases, the digital correction block can correct the result as long as the comparison level errors stay within $\pm V_{FS}/4$ resulting in comparison levels that stay within $\pm V_{FS}/2$.

5.4 Design Details

5.4.1 Architecture

Table 3 summarizes the main target specifications. The total resolution and the sampling rate are chosen as 9 bits and 100 MS/s, respectively.

Table 3: Target ADC specifications.

Process Technology	CMOS 0.18 μm
Core Size	$\leq 2 \times 2\,\text{mm}^2$
Power	$\leq 40\,\text{mA}$
Resolution	≥ 9 bit
Sampling rate	$\geq 100\,\text{MS/s}$
Etc.	• 3 stages total • Two ADCs interleaved with op-amp sharing • Foreground calibration only • Input bootstrapped switches to reduce sampling non-linearity

A top level block diagram is shown in Figure 53.

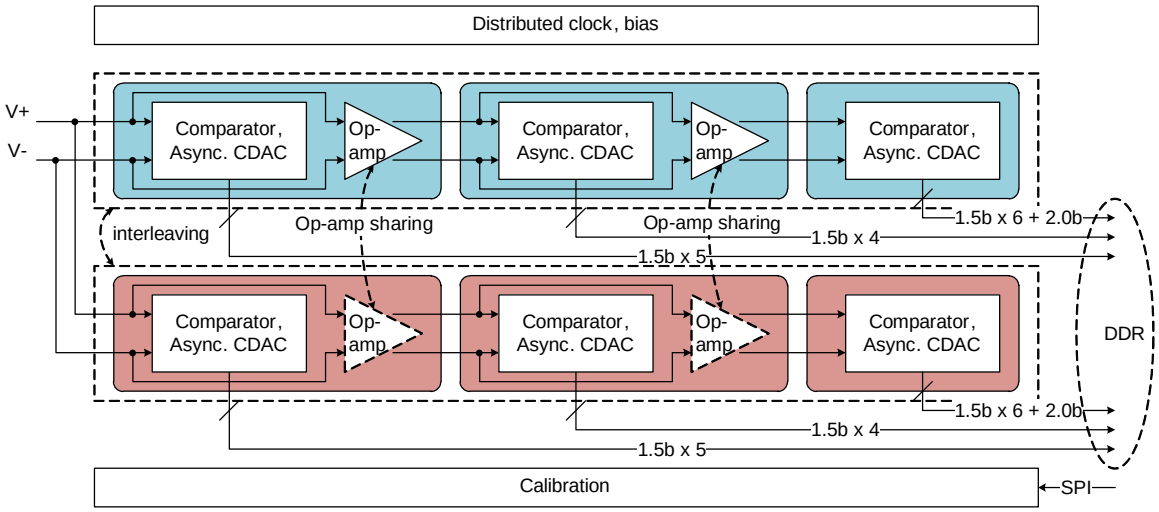


Figure 53: Block diagram of the proposed ADC.

Two independent but identical ADCs will be interleaved to reduce the speed

requirement. However, in order to avoid a power penalty, op amps will be shared between two paths. Only two op amps are required by the op-amp sharing scheme.

To provide ENOB of > 9 b, calibration may be required since component mismatches in monolithic integration usually limit the maximum accuracy to about 10 b [58]. The last stage is chosen to have $1.5 \times 6 + 2.0$ bits for the calibration. The total bits are

$$\begin{aligned}(\textit{total bits}) &= (1.5 \times 5 - 0.5 \times 4) + (1.5 \times 4 - 0.5 \times 3) - 1.5 \\ &= 5.5 + 4.5 - 1.5 \\ &= 8.5\end{aligned}$$

and the remaining bits will be used for calibration. Even though background calibration has been actively investigated recently [29, 59, 60], only a foreground calibration scheme similar to [61] will be used since the main idea of this work is not the calibration. Separate calibrations have to be performed for the two different paths. The last digital correction block will merge all digital outputs and apply the stored calibration data as well.

The input sampling switch may need bootstrapping if the target resolution is higher than 10 bits. Since it has been shown that conventional complementary switches attain, at best, -65 dBc track-mode distortion for a single-ended $0.8\,V_{pp}$ signal at the Nyquist input frequency of 25 MHz [55]. Since SNR is [38]

$$SNR = 6.02 \times ENOB + 1.76,$$

-65 dBc corresponds to about 10.5 bits maximum. Since the target of the proposed ADC is $>$ 9-bit accuracy, the bootstrapping scheme may be required, and the scheme in [62] will be used.

5.4.2 ASHMSAR Operations

Figure 54 shows the overall schematic of the proposed ASHMSAR.

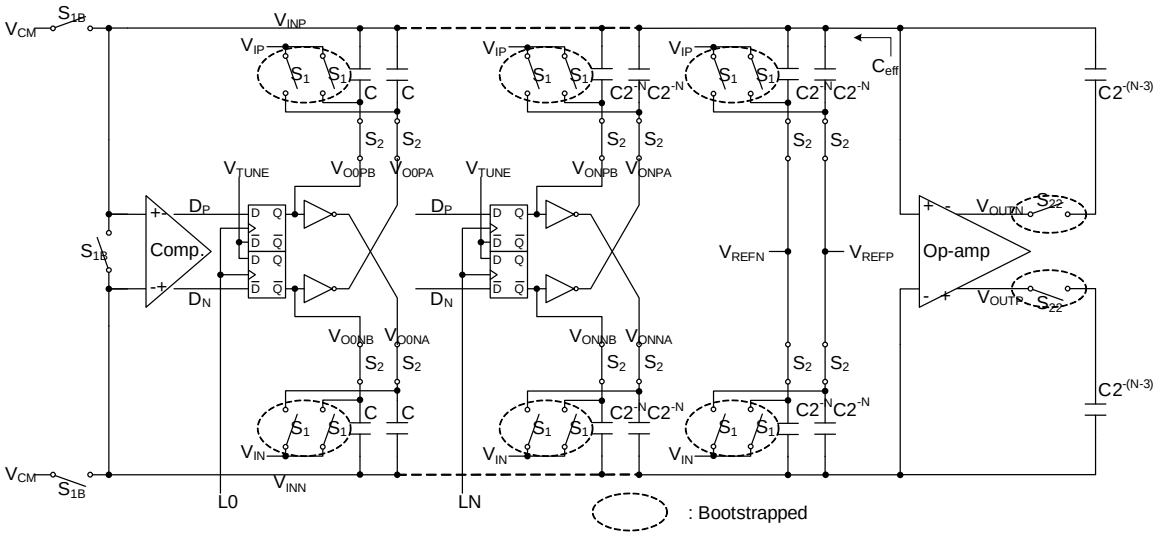


Figure 54: Schematic of ASHMSAR.

The ASHMSAR includes a preamplifier, a comparator followed by $N+1$ stages, dummy capacitors, and finally an op amp. The preamplifier amplifies the signal for the comparator, reduces the input-referred offsets, and operates in open-loop fashion to maximize bandwidth. The comparator is implemented as a simple "filter" circuit [63]. Even though this comparator implementation does not have sharp comparison characteristics, it has the advantage of reducing metastability by requiring at least a transistor threshold voltage difference between the signals. In Figure 54, for capacitor values, $C \approx 6.4\,\text{pF}$ is chosen for the 1st stage C value due to kT/C noise requirement, so $C_{eff} = 4C \approx 25.6\,\text{pF}$. The gain of amplifier is chosen as $A = C_{eff}/C2^{-(N-3)} = 4/2^{-(N-3)} = 2^{N-1}$, and since $N = 5$, $A = 16$ means the dynamic range for later stages will be reduced.

The variables in Figure 54 are defined as follows:

- V_{REFP}: positive reference voltage
- V_{REFN}: negative reference voltage
- $V_{FS} = V_{REFP} - V_{REFN}$: full-scale voltage

- $V_{CM} = \frac{V_{REFP}+V_{REFN}}{2}$: common-mode reference voltage
- $V_{ID} = V_{IP} - V_{IN}$: differential-mode input voltage
- V_{OUTP}: positive output voltage
- V_{OUTN}: negative output voltage
- V_{OUTD}: differential-mode output voltage
- The common-mode input voltage $\frac{V_{IP}+V_{IN}}{2}$ is assumed to be the same as the common-mode reference voltage, V_{CM}
- C_{eff}: effective total input capacitance

$$\begin{aligned} C_{eff} &= 2\left(C + \frac{C}{2} + \frac{C}{2^2} + \cdots + \frac{C}{2^N}\right) + 2\frac{C}{2^N} \\ &= 4C \end{aligned} \tag{17}$$

First, ASHMSAR starts with sampling depicted as in Figure 55.

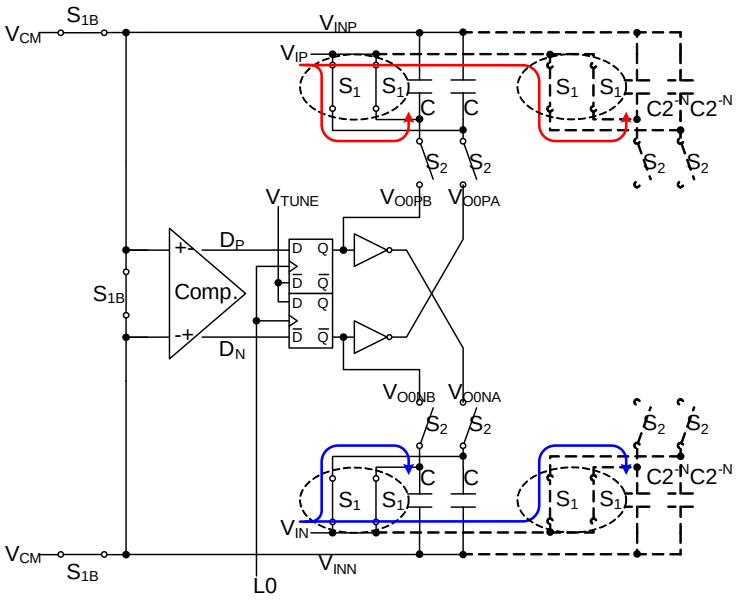


Figure 55: ASHMSAR at the sampling.

Two S_{1B} switches at V_{INP}, and V_{INN} are closed to the common-mode reference voltage V_{CM}, and the S_{1B} switch in between is also closed. The signal $L0, L1, \cdots LN = 0$ resets all the latches. Since the latches are implemented by latch-type voltage sense amplifiers, both Q and $\bar{Q}$ outputs become 1 at reset [64, 65]. The input signals V_{IP} and V_{IN} are sampled to capacitors with the total capacitance of $4C$ from (17) for each differential input node through the S_1 switches. As mentioned in Subsection 5.4.1, all S_1 switches are bootstrapped to minimize the distortion. Since all the latches are in the reset state,

$$\begin{cases} Q_{D_P} = 1 \rightarrow V_{O0PA} = V_{REFN} \\ Q_{D_N} = 1 \rightarrow V_{O0PB} = V_{REFP} \\ \bar{Q}_{D_P} = 1 \rightarrow V_{O0NA} = V_{REFN} \\ \bar{Q}_{D_N} = 1 \rightarrow V_{O0NB} = V_{REFP}. \end{cases}$$

Therefore, effective outputs are

$$\begin{cases} V_{O0P} = \frac{V_{O0PA}+V_{O0PB}}{2} = V_{CM} \\ V_{O0N} = \frac{V_{O0NA}+V_{O0NB}}{2} = V_{CM}. \end{cases} \tag{18}$$

Figure 56 shows the ASHMSAR at the start of the successive approximation ($t = t_0$ from Figure 59).

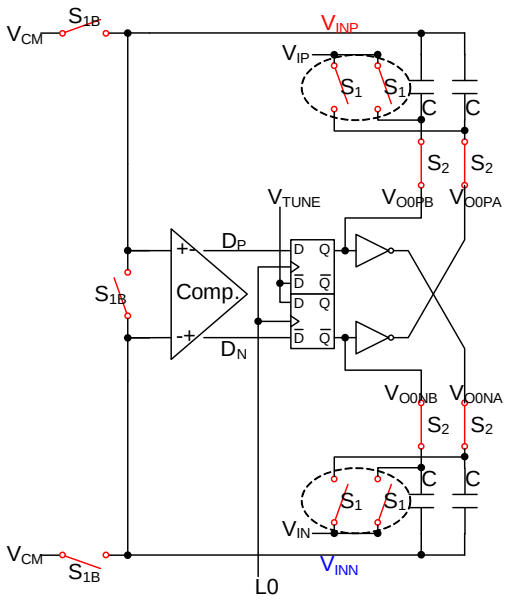


Figure 56: ASHMSAR at the start of the successive approximation.

S_{1B} switches open first to prevent signal-dependent charge injection [46], and this moment defines the sampling instant. The S_{1B} switch in between opens a bit after, thereby equalizing any charge mismatches between V_{INP} and V_{INN}. After some delay, the S_1 switches open, and this is the end of the sampling. Then, the S_2 switches close to connect the outputs of the latches to the capacitors for the successive approximation. Since the above sampling procedure flips the polarity, the node voltages V_{INP}, V_{INN} will approach

$$\begin{cases} V_{INP} \rightarrow 2V_{CM} - V_{IP} \\ V_{INN} \rightarrow 2V_{CM} - V_{IN}. \end{cases}$$

Assuming $V_{INP} > V_{INN}$ after some delay, preamplifier outputs are $V_{PREP} > V_{PREN}$, so $D_P = 1$ and $D_N = 0$ ($t = t_{0C}$ from Figure 59).

When the $L0$ signal goes high at $t = t_1$, the latches will hold D_P, D_N values. Since

$Q = 1$ and $\bar{Q} = 0$ for the D_P latch, and $Q = 0$ and $\bar{Q} = 1$ for the D_N latch,

$$\begin{cases} Q_{D_P} = 1 \rightarrow V_{O0PA} = V_{REFN} \\ Q_{D_N} = 0 \rightarrow V_{O0PB} = V_{REFN} \\ \bar{Q}_{D_P} = 0 \rightarrow V_{O0NA} = V_{REFP} \\ \bar{Q}_{D_N} = 1 \rightarrow V_{O0NB} = V_{REFP}. \end{cases}$$

Therefore, effective outputs are

$$\begin{cases} V_{O0P} = \frac{V_{O0PA}+V_{O0PB}}{2} = V_{REFN} \\ V_{O0N} = \frac{V_{O0NA}+V_{O0NB}}{2} = V_{REFP}. \end{cases}$$

This operation is shown in Figure 57.

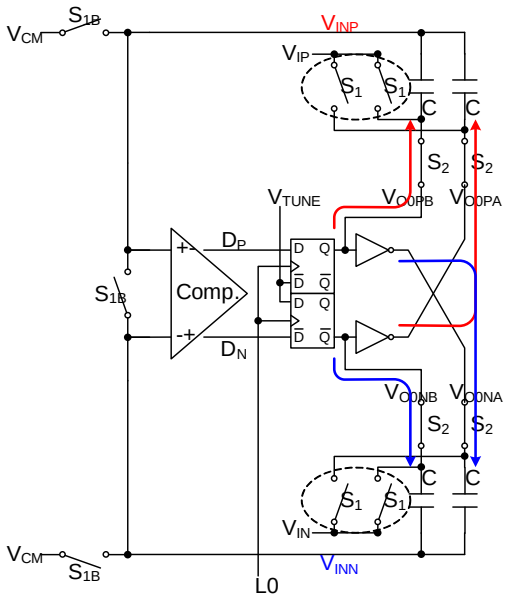


Figure 57: ASHMSAR at the evaluation.

Because of the charge conservation, the above changes have the effect of adding a total charge of

$$\begin{aligned} 2C\left(V_{REFN} - V_{CM}\right) &= 2C \times \frac{2V_{REFN} - V_{REFP} - V_{REFN}}{2} \\ &= C\left(V_{REFN} - V_{REFP}\right) \end{aligned}$$

to the node V_{INP} and adding a total charge of

$$\begin{aligned} 2C\left(V_{REFP}-V_{CM}\right) &= 2C\times\frac{2V_{REFP}-V_{REFP}-V_{REFN}}{2} \\ &= C\left(V_{REFP}-V_{REFN}\right) \end{aligned}$$

to the node V_{INN}. Since each node has the equivalent capacitance of $4C$, the new V_{INP} and V_{INN} are

$$\begin{cases} V_{INP} = \dfrac{4C\left(2V_{CM}-V_{IP}\right)+C\left(V_{REFN}-V_{REFP}\right)}{4C} \\ \qquad\quad = 2V_{CM}-V_{IP}+\dfrac{V_{REFN}-V_{REFP}}{4} \\ \\ V_{INN} = \dfrac{4C\left(2V_{CM}-V_{IN}\right)+C\left(V_{REFP}-V_{REFN}\right)}{4C} \\ \qquad\quad = 2V_{CM}-V_{IN}+\dfrac{V_{REFP}-V_{REFN}}{4}. \end{cases}$$

In other words, $V_{IND}=V_{INP}-V_{INN}$ is

$$\begin{aligned} V_{IND} &= 2V_{CM}-V_{IP}+\frac{V_{REFN}-V_{REFP}}{4}-2V_{CM}+V_{IN}-\frac{V_{REFP}-V_{REFN}}{4} \\ &= -V_{ID}-\frac{V_{REFP}-V_{REFN}}{2} \\ &= -V_{ID}-\frac{V_{FS}}{2}. \end{aligned}$$

Therefore, this operation has the effect of subtracting $\frac{V_{FS}}{2}$ from $-V_{ID}$. This is the end of the first-stage successive approximation of the ASHMSAR.

Figure 58 shows the ASHMSAR at the start of the second successive approximation.

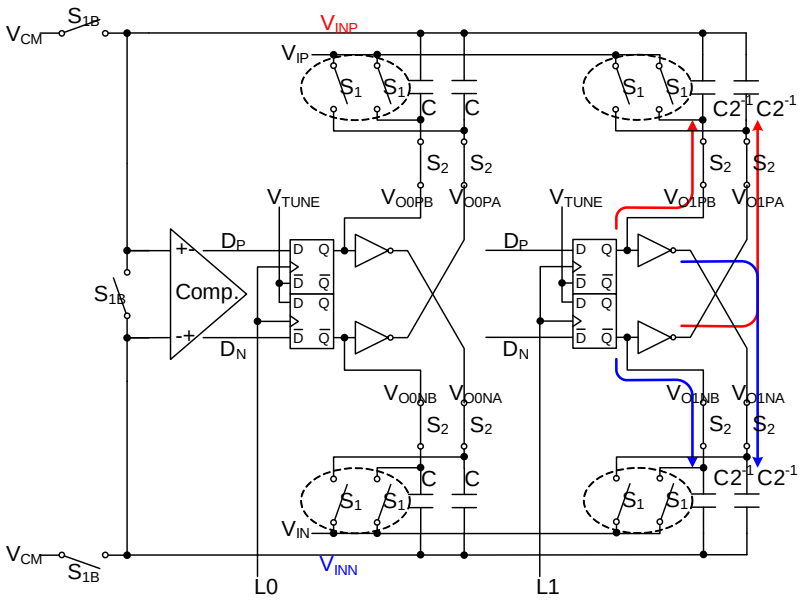


Figure 58: ASHMSAR at the start of the second successive approximation.

Assuming $V_{INN} > V_{INP}$ after some delay at this time, the preamplifier outputs are $V_{PREN} > V_{PREP}$, so $D_P = 0$ and $D_N = 1$ ($t = t_{1C}$ from Figure 59).

The self-timed logic generates an internal trigger for L_1, and V_{O1P} and V_{O1N} are evaluated according to D_P, D_N. When $L1$, which is the delayed $L0$ signal, goes high at $t = t_2$ (from Figure 59), the latches will hold D_P, D_N values. Since $Q = 0$ and $\bar{Q} = 1$ for the D_P latch, and $Q = 1$ and $\bar{Q} = 0$ for the D_N latch,

$$\begin{cases} Q_{D_P} = 0 \rightarrow V_{O1PA} = V_{REFP} \\ Q_{D_N} = 1 \rightarrow V_{O1PB} = V_{REFP} \\ \bar{Q}_{D_P} = 1 \rightarrow V_{O1NA} = V_{REFN} \\ \bar{Q}_{D_N} = 0 \rightarrow V_{O1NB} = V_{REFN}. \end{cases}$$

Therefore, effective outputs are

$$\begin{cases} V_{O1P} = \frac{V_{O1PA}+V_{O1PB}}{2} = V_{REFP} \\ V_{O1N} = \frac{V_{O1NA}+V_{O1NB}}{2} = V_{REFN}. \end{cases}$$

Following the same calculations as above,

$$V_{IND} = -V_{ID} - \frac{V_{FS}}{2} + \frac{V_{FS}}{4}$$

If the preamplifier outputs are $V_{PREN} \approx V_{PREP}$ [1], then latches will hold $D_P = 0$ and $D_N = 0$. Since $Q = 0$ and $\bar{Q} = 1$ for the D_P latch, and $Q = 0$ and $\bar{Q} = 1$ for the D_N latch,

$$\begin{cases} Q_{D_P} = 0 \rightarrow V_{O1PA} = V_{REFP} \\ Q_{D_N} = 0 \rightarrow V_{O1PB} = V_{REFN} \\ \bar{Q}_{D_P} = 1 \rightarrow V_{O1NA} = V_{REFN} \\ \bar{Q}_{D_N} = 1 \rightarrow V_{O1NB} = V_{REFP} \end{cases}$$

and effective outputs are

$$\begin{cases} V_{O1P} = \frac{V_{O1PA}+V_{O1PB}}{2} = V_{CM} \\ V_{O1N} = \frac{V_{O1NA}+V_{O1NB}}{2} = V_{CM} \end{cases}$$

which is the same as (18). Therefore, there will be neither subtraction nor addition.

In general, after the final $N+1$-th stage, the output is

$$V_{IND} = -V_{ID} + \sum_{k=0}^{N} d_k \frac{V_{FS}}{2^{k+1}}, \tag{19}$$

where $d_k = -1, 0$ or 1 is the k-th digitized value since the decision is always in the direction of reducing $|V_{ID}|$.

Figure 59 shows the first and the second successive approximation timing diagram.

[1] This case is the metastability case discussed in Subsection 5.3.2

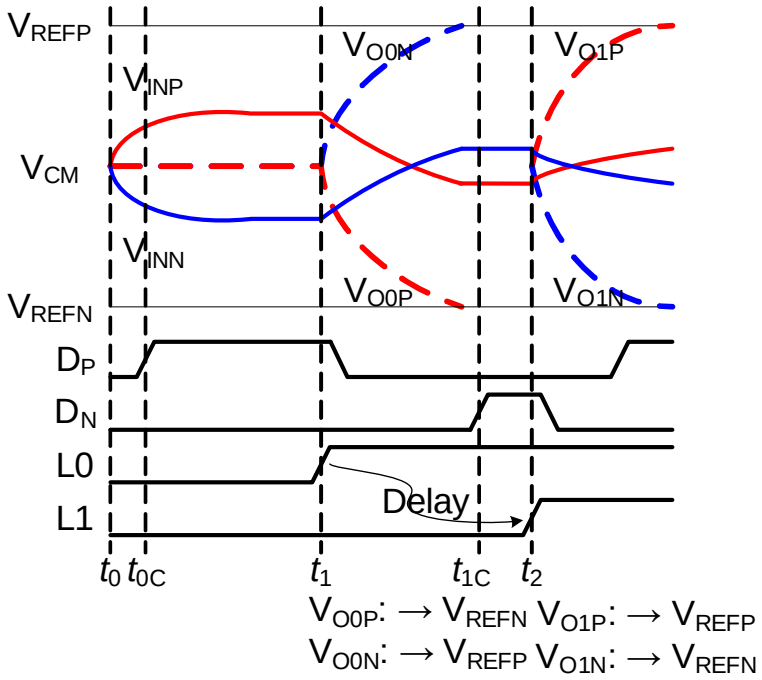


Figure 59: ASHMSAR successive approximation timing diagram.

After the final $N+1$-th stage, the residue signal is amplified, as shown in Figure 60.

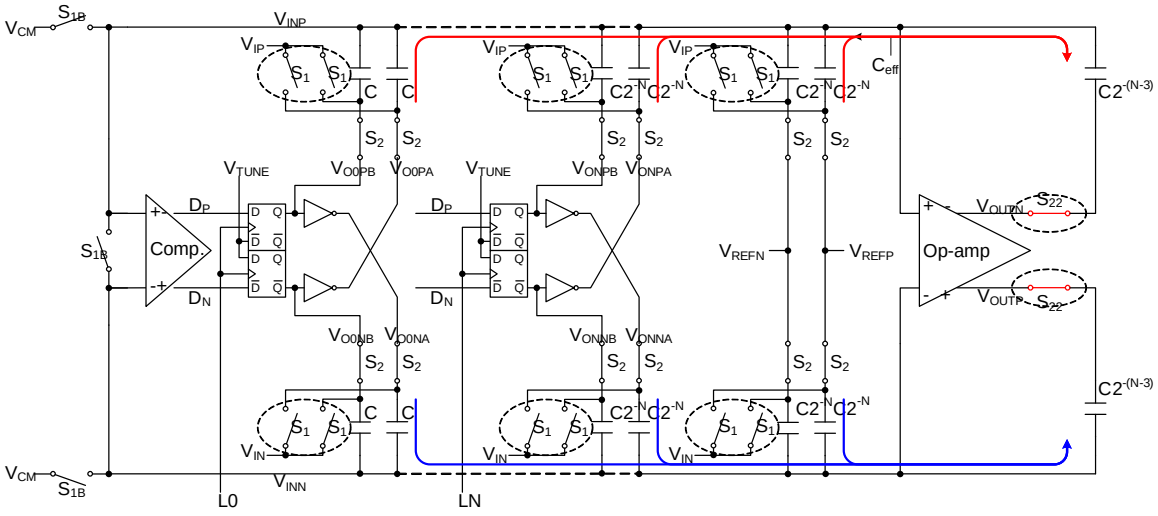


Figure 60: ASHMSAR amplification stage.

First, the S_{22} switches close to connect the op-amp outputs to the capacitors. The

op-amp closed-loop gain is

$$\begin{aligned} G &= \frac{C_{eff}}{\frac{C}{2^{N-2}}} \\ &= \frac{4C \times 2^{N-2}}{C} \\ &= 2^N \end{aligned} \tag{20}$$

Here, the feedback capacitor is chosen to be $C2^{-(N-2)}$ to reduce the dynamic range by half for the next stage so that op-amp specifications can be relaxed. The S_{22} switches are bootstrapped to reduce distortion.

From (19), (20), the final output at the end of amplification is

$$\begin{aligned} V_{OUTD} &= V_{OUTP} - V_{OUTN} \\ &= GV_{IND} \\ &= 2^N \left(-V_{ID} + \sum_{k=0}^{N} d_k \frac{V_{FS}}{2^{k+1}} \right) \\ &= -V_{ID}2^N + \sum_{k=0}^{N} d_k V_{FS} 2^{N-k-1}. \end{aligned}$$

In other words, the proposed ASHMSAR can not only sample-and-hold (S/H), but also digitize, subtract, and then amplify in sequence with proper timing.

5.4.3 Operational Amplifier

A two-stage op amp with Miller compensation as in Figure 61 is designed for the amplifier.

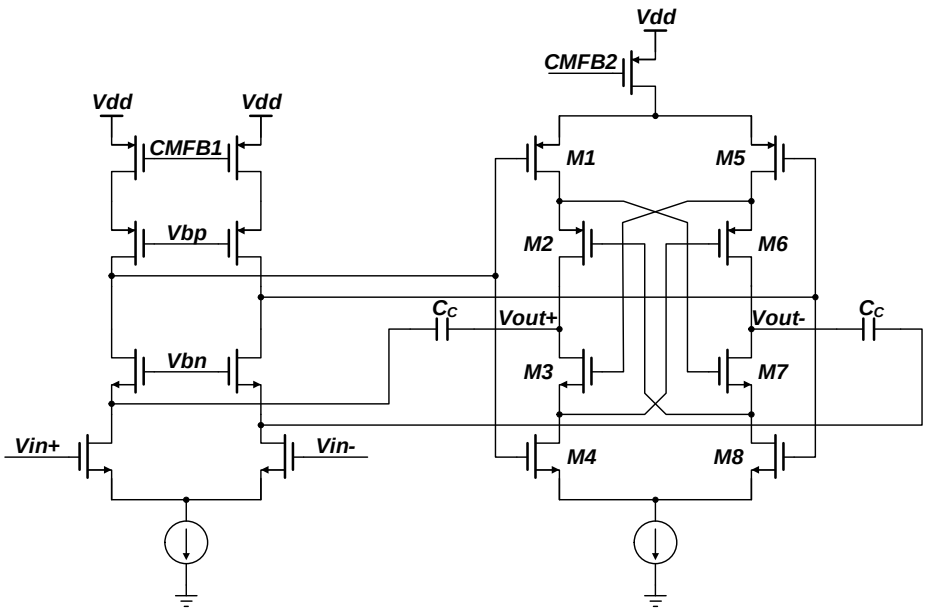


Figure 61: Two-stage op amp with a feedforward-regulated cascode for the 2nd stage.

The first stage is a conventional cascode, and the second stage is a feedforward-regulated cascode [66].

For the second stage,

$$\begin{aligned} R_{out} &\approx (2g_{m2}r_{o2}r_{o1})||(2g_{m3}r_{o3}r_{o4}) \\ &\approx g_{m2}r_{o2}r_{o1} \end{aligned} \tag{21}$$

by ignoring parasitics [66]. Since $G_m \approx g_{m1} + g_{m4}$, the second stage direct current (DC) gain can be approximated as the following equation using (21) [46].

$$\begin{aligned} A_{0,2nd} &\approx G_m R_{out} \\ &= (g_{m1} + g_{m4})g_{m2}r_{o2}r_{o1} \end{aligned}$$

Capacitors C_c are Miller compensation capacitors, and signals are returned to the cascode nodes to eliminate right half-plane (RHP) zero by eliminating feedforward paths [67].

The final settling behavior of the designed op amp is shown in Figure 62 by transient simulation. The input capacitors of the SC circuit are charged to 46.875 mV

differentially to generate the maximum output swing of $46.875 \times 16 = 750\,(\mathrm{mV})$. The output settles within the desired settling accuracy of 2^{-7} in 3.185 ns. With a feedback factor of $\beta = 1/16$, the DC gain is 45.53 dB, and the unity gain frequency is 197.7 MHz with a phase margin (PM) of 67.54 °.

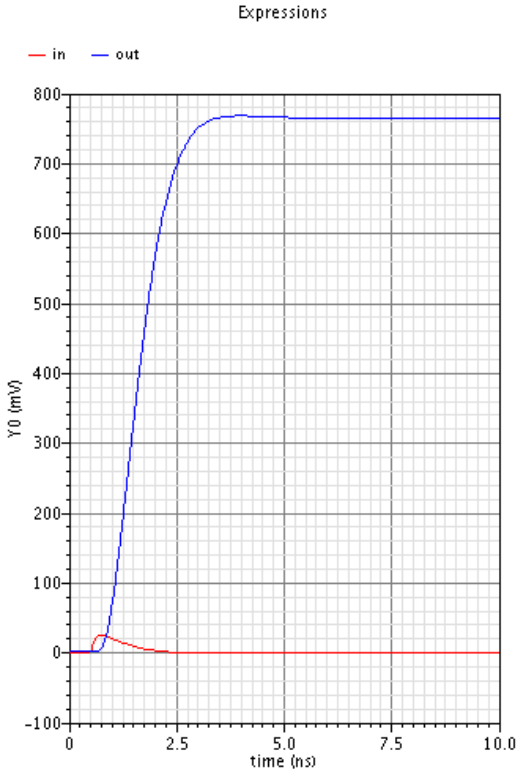


Figure 62: ASHMSAR amplification stage.

5.4.4 Delay Calculation

In Subsection 5.4.2, it was shown that t_2 should have a certain amount of delay from t_1. Then, minimum delay should be calculated, which is necessary to guarantee the requirement discussed in Subsection 5.3.2. The following parameters are defined first for the calculation of this requirement. For simplicity, the DAC output driver, the preamplifier, and the op amp are approximated with the dominant-pole model.

- τ_{DAC}: DAC output driver time constant

- τ_{PRE}: preamplifier time constant
- V_{COMP}: comparator threshold
- A_0: preamplifier DC gain
- k: k-th stage (k=$0, 1, \cdots, N-1$)

The minimum delay required τ_{min} can be broken down into two components: τ_1 for the DAC settling, and τ_2 for the preamplifier amplification.

When τ_1 is considered for the k-th stage, both V_{INP}, V_{INN} have to settle within $V_{FS}/2^{k+3}$, respectively, for the $V_{IND} = V_{INP} - V_{INN}$ to settle within $V_{FS}/2^{k+2}$. Since the DAC gain for the k-the stage is $1/2^{k+1}$ from (19), differential voltages V_{OkP}, V_{OkN} have to settle within $V_{FS}/2^{k+3} \times 2^{k+1} = V_{FS}/2^2$ from $V_{FS}/2$. Therefore,

$$\begin{aligned} &\frac{V_{FS}}{2} e^{-\tau_1/\tau_{DAC}} = \frac{V_{FS}}{2^2} \\ &\therefore \tau_1 \leq \tau_{DAC} \ln 2. \end{aligned} \tag{22}$$

Even though this calculation assumes an error of $V_{FS}/4$ for τ_1 without margin, since the preamplifier may start earlier in practice so that τ_1 may overlap with τ_2, this calculation implicitly includes some margin.

If the preamplifier amplification time is τ_2, the preamplifier is reset during the τ_1 period and starts at the end of the τ_1 period. For the k-th stage, the minimum input level, which should be amplified enough to overcome the comparator threshold, is $V_{FS}/2^{k+2}$. Therefore,

$$\begin{aligned} &A_0 \left(1 - e^{-\tau_2/\tau_{PRE}}\right) \left(\frac{V_{FS}}{2^{k+2}}\right) = V_{COMP} \\ &\therefore \tau_2 \leq -\tau_{PRE} \ln \left(1 - \frac{V_{COMP} 2^{k+2}}{V_{FS} A_0}\right). \end{aligned}$$

Let's assume

$$\begin{cases} V_{COMP} = V_{FS}/2 \\ A_0 = 2^{\alpha} \end{cases}$$

Then,

$$\begin{aligned}\tau_2 &\leq -\tau_{PRE} \ln\left(1 - \frac{2^{k+2}}{2 \cdot 2^{\alpha}}\right) \\ &= -\tau_{PRE} \ln\left(1 - \frac{2^{k+1}}{2^{\alpha}}\right) \\ &= \tau_{PRE} \ln\left(\frac{2^{\alpha}}{2^{\alpha} - 2^{k+1}}\right)\end{aligned}$$

Interestingly, if $\alpha \leq N + 1$, τ_2 may approach infinity or may be not well defined. In other words, the preamplifier output may never reach the threshold level. Therefore,

$$A_0 > 2^{N+1}$$

is another requirement for the preamplifier. If

$$A_0 = 2^{N+2}$$

is chosen considering some margin, then

$$\begin{aligned}\tau_2 &\leq \tau_{PRE} \ln\left(\frac{2^{N+2}}{2^{N+2} - 2^{k+1}}\right) \\ &= \tau_{PRE} \ln\left(\frac{2^{N+1}}{2^{N+1} - 2^{k}}\right) \\ &\leq \tau_{PRE} \ln\left(\frac{2^{N+1}}{2^{N+1} - 2^{N}}\right) \\ &= \tau_{PRE} \ln 2\end{aligned} \tag{23}$$

Figure 63 shows the timing diagram for the above calculations.

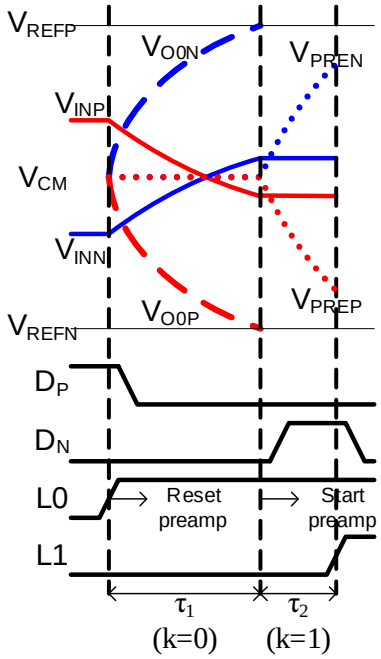


Figure 63: Preamplifier delay.

From (22),(23), the total conversion time for the ASHMSAR will be

$$
\begin{aligned}
\tau_{total} &= \sum_{k=0}^{N} \tau_{k-th\ stage} + \tau_{amp} \\
&= \sum_{k=0}^{N} (\tau_{1,k} + \tau_{2,k}) + \tau_{amp} \\
&\leq (N+1)\tau_{DAC} \ln 2 + \tau_{PRE} \sum_{k=0}^{N} \ln \left(\frac{2^{N+1}}{2^{N+1} - 2^k} \right) + \tau_{amp} \\
&= (N+1)\tau_{DAC} \ln 2 - \tau_{PRE} \sum_{k=0}^{N} \ln \left(1 - \frac{1}{2^{N+1-k}} \right) + \tau_{amp} \\
&= (N+1)\tau_{DAC} \ln 2 - \tau_{PRE} \sum_{k=1}^{N+1} \ln \left(1 - \frac{1}{2^k} \right) + \tau_{amp} \\
&= (N+1)\tau_{DAC} \ln 2 - \tau_{PRE} \ln \prod_{k=1}^{N+1} \left(1 - \frac{1}{2^k} \right) + \tau_{amp} \\
&\leq (N+1)\tau_{DAC} \ln 2 - \tau_{PRE} \ln \prod_{k=1}^{\infty} \left(1 - \frac{1}{2^k} \right) + \tau_{amp} \\
&\leq (N+1)\tau_{DAC} \ln 2 - \tau_{PRE} \ln Q + \tau_{amp}
\end{aligned}
$$

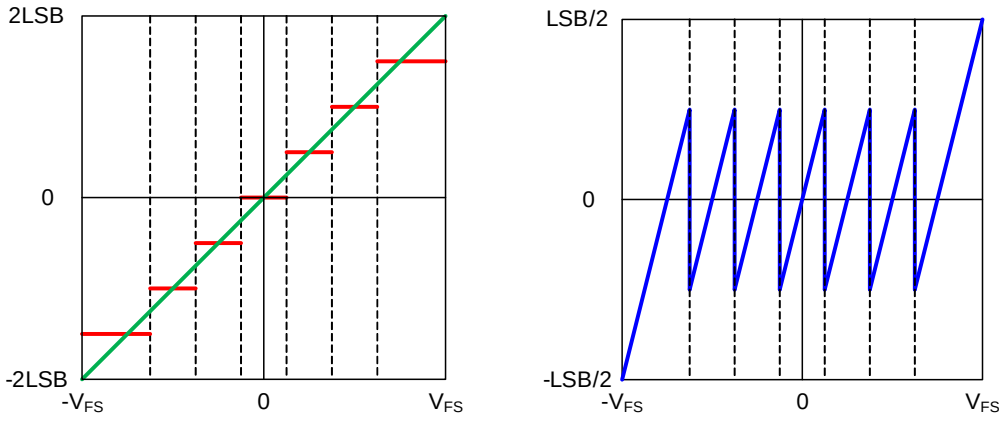
where $Q = \prod_{k=1}^{\infty}\left(1-\frac{1}{2^k}\right)$ is one of the digital search tree constants [68] and converges to an irrational number $0.2887880950\ldots$. Since the final amplification stage requires $2^{-(N_{total}-N-1)}$ accuracy, it requires $(N_{total}-N-1)\tau_{op-amp}\ln 2$ settling time. Therefore,

$$\begin{aligned}\tau_{total} &\le (N+1)\tau_{DAC}\ln 2 + \tau_{PRE}\ln\frac{1}{Q} + (N_{total}-N-1)\tau_{op-amp}\ln 2\\ &= \left[N_{total}-(N+1)\left(1-\frac{\tau_{DAC}}{\tau_{op-amp}}\right)\right]\tau_{op-amp}\ln 2 + \tau_{PRE}\ln\frac{1}{Q}\\ &\approx \left[N_{total}-(N+1)\left(1-\frac{\tau_{DAC}}{\tau_{op-amp}}\right)\right]\tau_{op-amp}\ln 2 + \tau_{PRE}\ln 3.463.\end{aligned}$$

The above calculations show that the intermediate output V_{IND} does not have to settle within $2^{-(N_{total}-N-1)}$ accuracy. This accuracy is required only for the final amplification stage. Also, τ_{PRE} related time has a constant maximum of $\tau_{PRE}\ln\frac{1}{Q}$ independent of N and N_{total}, and $\tau_{DAC} < \tau_{op-amp}$ is required to reduce the conversion time.

5.4.5 Calibration

The linear gain stage error is corrected by digitally modifying the weight of each bit decision as described in [28]. For the sake of simplicity, the input and digital output transfer curve of a 2.5 bit example is shown in Figure 64(a), and the residue plot (i.e. $(input)-(digital)$) is shown in Figure 64(b).



(a) (b)

Figure 64: Ideal case plot of (a) input and output, and (b) residue.

If there is any error in the weight of each bit, the digital output deviates from its ideal value, which means that the residue will deviate from its ideal value as well, as shown in Figure 65. The error should not exceed LSB/2 for the calibration algorithm to function if the radix of each bit is exactly 2 as illustrated in this example [28]. In real implementation, a margin of more than 25 % for the radix is designed for each bit.

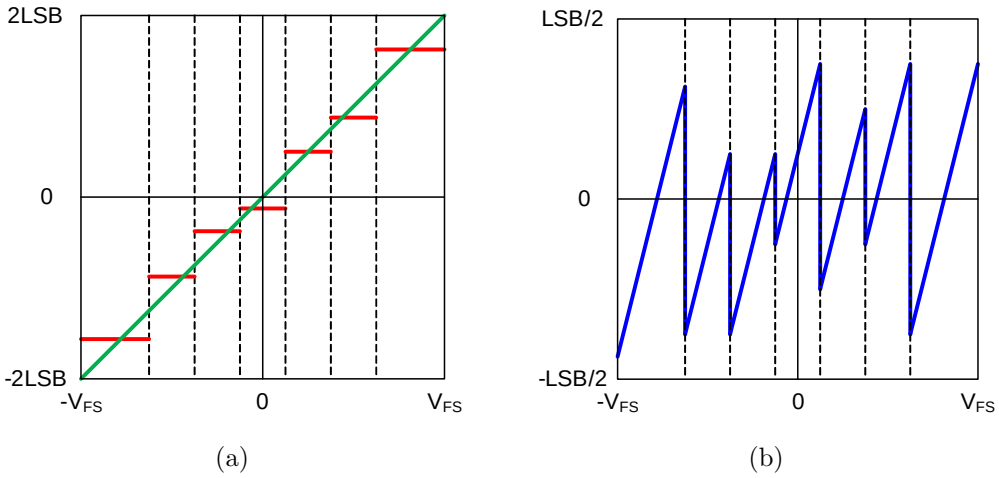
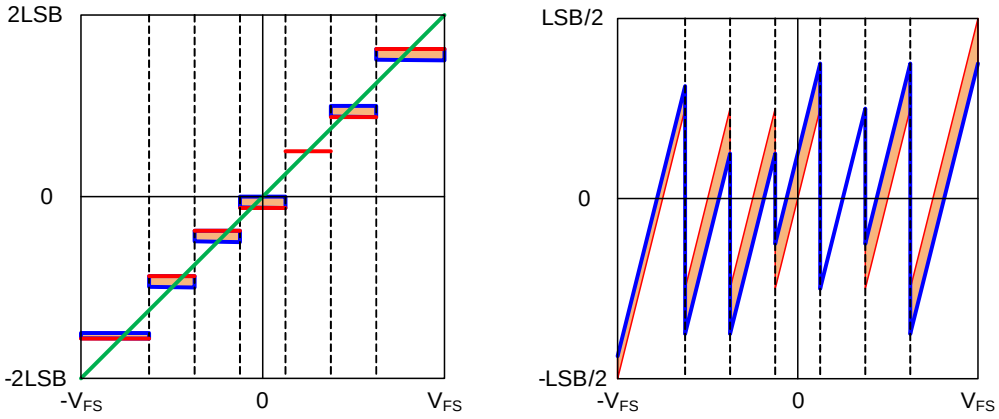


Figure 65: Plot of (a) input and output, and (b) residue when bit weight error occurs.

The residue errors are measured by the final stage, and then correction values are added digitally to the digital output values. Then the original ideal value can be recovered as shown in Figure 66.



(a) (b)

Figure 66: Plot of (a) input and output, and (b) residue after calibration.

On top of the linear error calibration as described above, the 2nd order and the 3rd order errors are also calibrated based on digital domain error compensation [29, 69].

Because

$$x = 2\sqrt{-\frac{1}{3p_2}}\cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{V_{res1}}{2\sqrt{-\frac{1}{27p_2}}}\right)\right] \tag{24}$$

is the solution of the reduced cubic equation

$$p_2 x^3 + x = V_{res1},$$

by defining $e(V_{res1}) \triangleq V_{res1} - x$,

$$p_2(V_{res1} - e(V_{res1}))^3 = e(V_{res1})$$

has to be satisfied with (24). In other words,

$$a_3\left(\frac{V_{res1} - e(V_{res1})}{2^3 - \Delta}\right)^3 = e(V_{res1})$$

is satisfied with [29]

$$e(V_{res1}) = V_{res1} - 2\sqrt{-\frac{1}{3p_2}}\cos\left[\frac{\pi}{3} + \frac{1}{3}\cos^{-1}\left(\frac{V_{res1}}{2\sqrt{-\frac{1}{27p_2}}}\right)\right], \tag{25}$$

$$p_2 \triangleq \frac{a_3}{(2^3 - \Delta)^3}. \tag{26}$$

For the 2nd order correction,

$$a_2 \left(\frac{V_{res1} - e(V_{res1})}{2^3 - \Delta} \right)^2 = e(V_{res1})$$

is satisfied with

$$e(V_{res1}) = V_{res1} + \frac{1 - \sqrt{1 + 4p_1 V_{res1}}}{2p_1}, \tag{27}$$

$$p_1 \triangleq \frac{a_2}{(2^3 - \Delta)^2}. \tag{28}$$

Therefore, (25) and (27) terms are added digitally at the final output with calibration parameters p_1, p_2 from (26) and (28).

5.5 Simulation Results

Since a simulation of the entire design is too time consuming to simulate, each individual stage is simulated separately to verify the performance.

Figure 67 shows the simulation results of the 1st stage residue with the Cadence Spectre [2] circuit simulator.

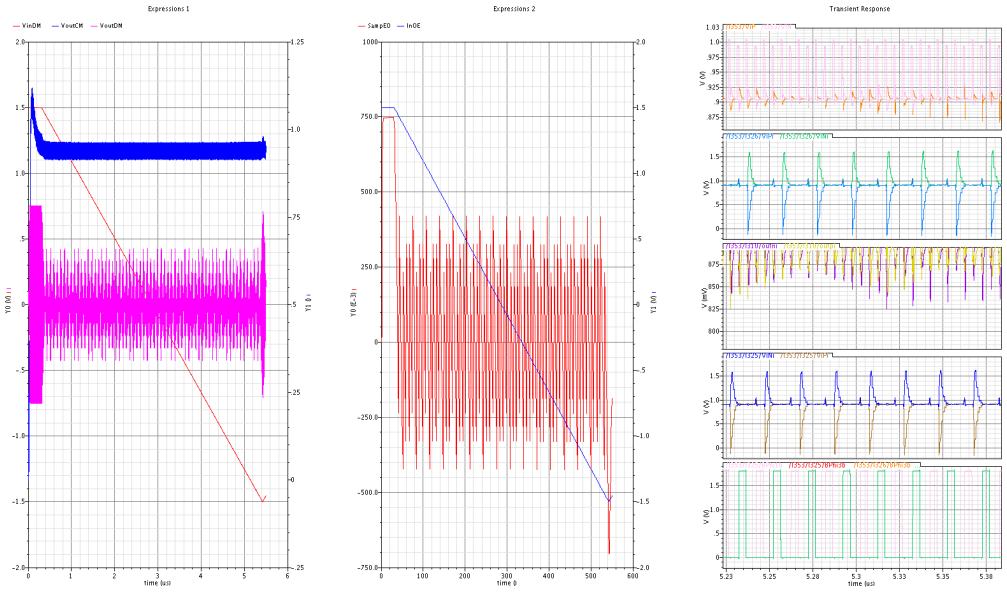
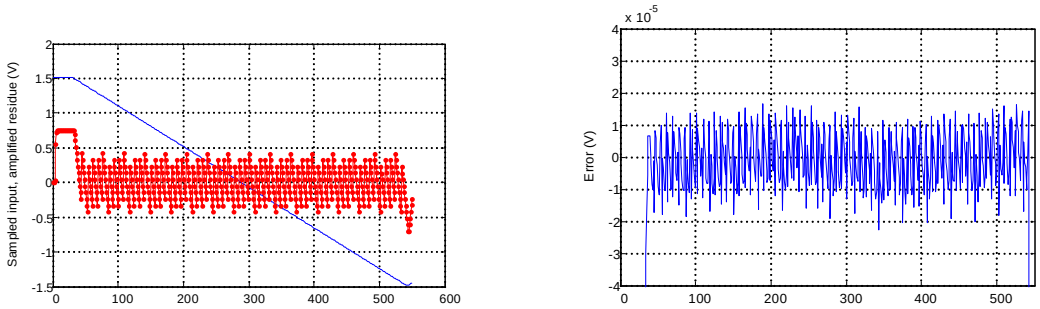


Figure 67: Schematic simulation result of the 1st stage.

[2]Cadence Spectre is a registered trademark of Cadence Design Systems, Inc.

From the simulation result of Figure 67, the final input and residue voltages at every clock cycle are extracted and plotted in Figure 68(a) using MATLAB. Then, the error voltages from the ideal values are calculated and plotted in Figure 68(b). In both cases, the x-axis represents the digital output code.



(a) (b)

Figure 68: First stage simulation result of (a) the input (solid line) and the residue (line with squares), and (b) the error voltage.

Figure 68(b) shows that the absolute value of error voltage is less than 2×10^{-5}. Since the single-ended full-scale voltage $V_{FS,single-ended}$ is 1.5 V,

$$2 \times 10^{-5} < \frac{1.5}{2^{16}} \approx 2.289 \times 10^{-5}.$$

In other words, the first stage satisfies the error requirement even without the calibration. However, this is only a simulation result, so calibration may still be necessary to secure enough margin.

Figure 69 shows the simulation result of the 2nd stage.

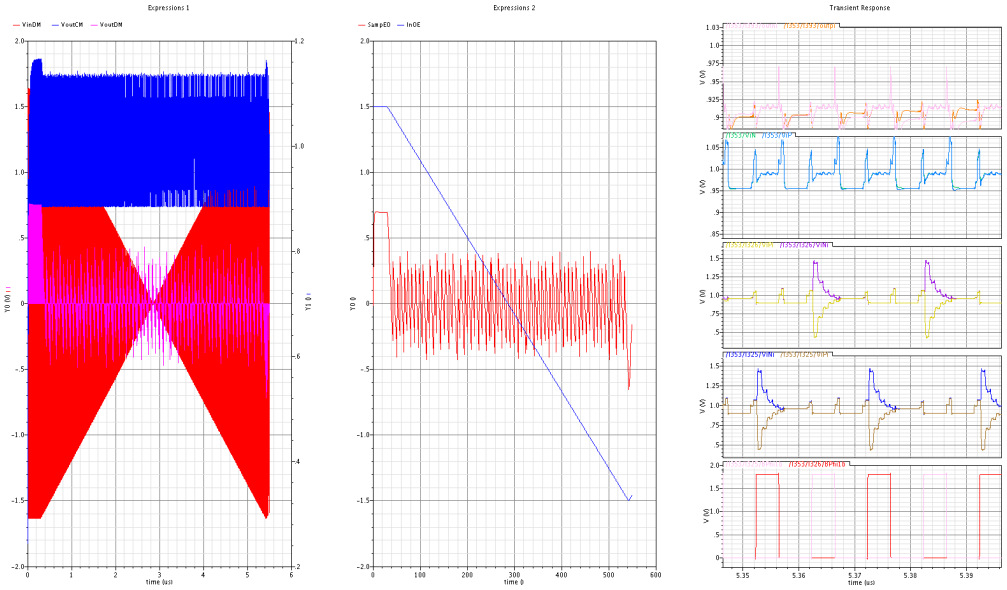
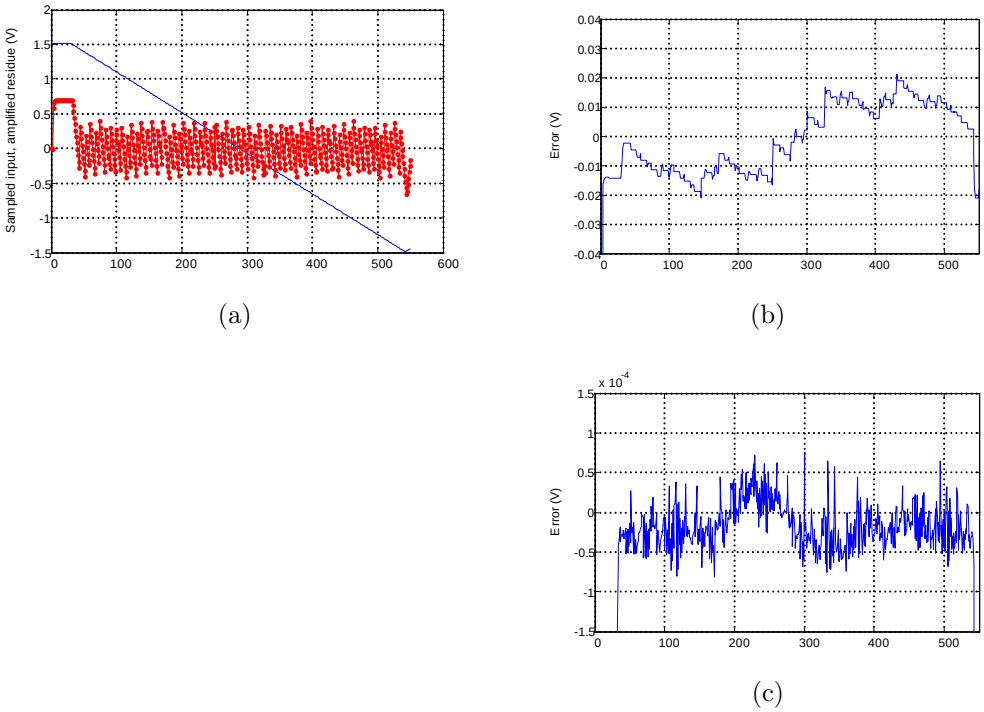


Figure 69: Schematic simulation result of the 2nd stage.

From the simulation result of Figure 69, the final input and residue voltages at every clock cycle are extracted and plotted in Figure 70(a) using MATLAB. Then, the error voltages are calculated and plotted in Figure 70(b).



(a) (b) (c)

Figure 70: The second stage simulation result of (a) the input (solid line) and the residue (line with squares), (b) the error voltage before calibration, and (c) the error voltage after calibration.

From Figure 70(b), the absolute value of the error voltage is about 20×10^{-3}, and

$$20 \times 10^{-3} < \frac{1.5}{2^6} \approx 23.44 \times 10^{-3}.$$

Therefore, the residue is accurate only to $V_{FS,single-ended}/2^6$ level, which is not sufficient. The large 2nd stage error is due mainly to its $C - 2C$ configuration. The first stage is implemented as a conventional binary weighted capacitor DAC. However, the implementation of a conventional binary weighted capacitor DAC for the 2nd stage will result in too small a unit capacitor size, and this implementation is impractical since the capacitor size has a minimum requirement due to fabrication accuracy. If the minimum size capacitor is chosen for the unit capacitor to implement a conventional capacitor DAC array, then the total capacitance will be unnecessarily large. Therefore, the $C - 2C$ configuration is chosen, but the $C - 2C$ configuration

is sensitive to the parasitics at the floating nodes, and these parasitics are mainly responsible for the large errors in Figure 70(b).

After the calibration algorithm described in Subsection 5.4.5 is performed by MATLAB, the error voltages are reduced as in Figure 70(c). New error voltages are less than

$$1 \times 10^{-4} < \frac{1.5}{2^{13}} \approx 183.1 \times 10^{-6}.$$

Therefore, the error is small enough to satisfy the requirement.

Figure 71 shows the simulation result of the 3rd stage.

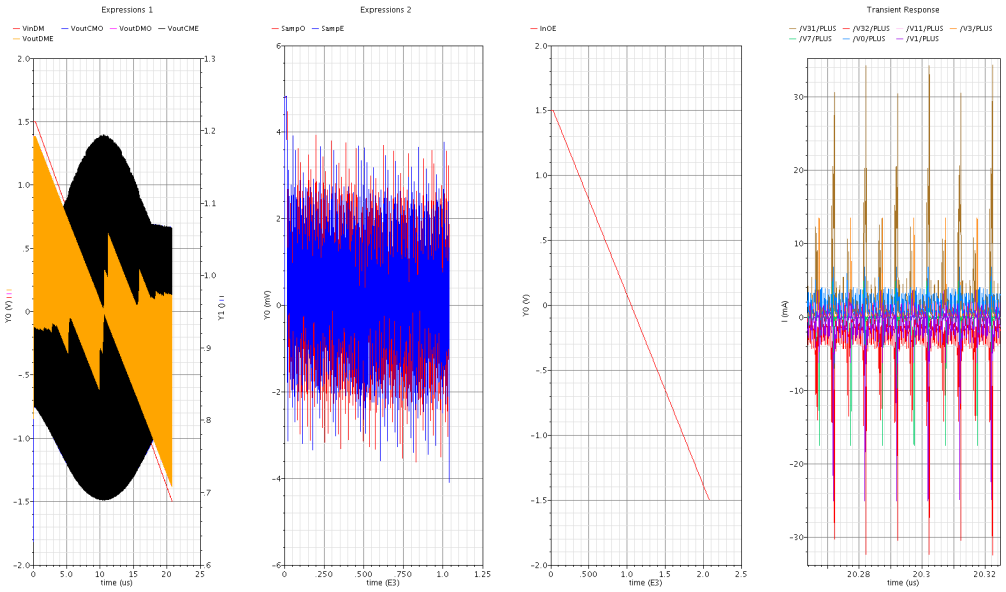
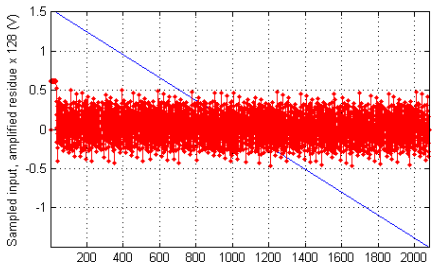
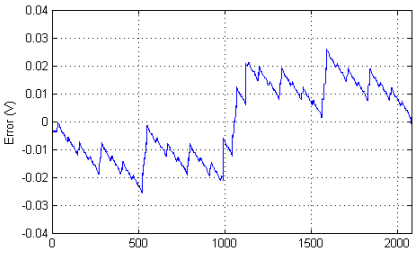


Figure 71: Schematic simulation result of the 3rd stage.

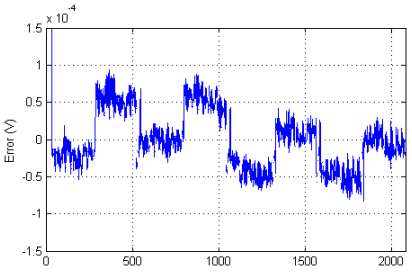
From the simulation result of Figure 71, final input and residue voltages at every clock cycle are extracted and plotted (Figure 72(a)) using MATLAB. Then, error voltages are calculated and plotted (Figure 72(b)).



(a)



(b)



(c)

Figure 72: The third stage simulation result of (a) the input (solid line) and the residue (line with squares), (b) the error voltage before calibration, and (c) the error voltage after calibration.

Figure 72(b) shows that the error voltage is as large as 25×10^{-3} level, which is about $V_{FS,single-ended}/2^5$ accuracy as follows:

$$25 \times 10^{-3} < \frac{1.5}{2^5} \approx 46.88 \times 10^{-3}.$$

The large 3rd stage error is due mainly to its $C - 2C$ configuration as described for the 2nd stage. Since the error voltages do not satisfy the target requirements, the calibration is performed as for the 2nd stage, and the error voltages are reduced as in Figure 72(c) after the calibration. After the calibration,

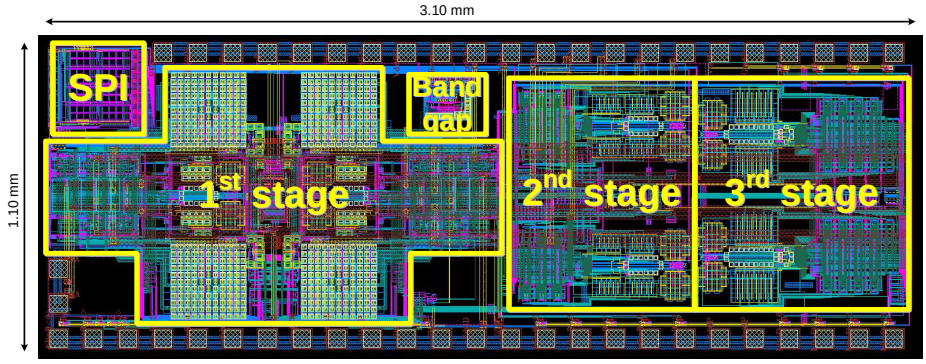
$$1 \times 10^{-4} < \frac{1.5}{2^{13}} \approx 183.1 \times 10^{-6},$$

and the new error voltages satisfy the target requirements.

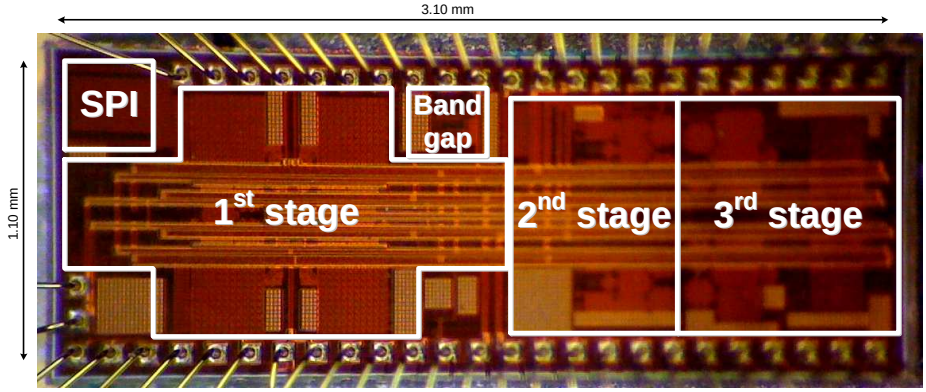
Therefore, all simulation results verify that the design satisfies the target requirements.

5.6 Evaluation

The layout is shown in Figure 73(a), and the ADC was fabricated in a 0.18-μm CMOS technology process. A die micrograph is shown in Figure 73(b). The die size is 3.10 mm $\times$ 1.10 mm.



(a)



(b)

Figure 73: ADC with ASHMSAR test chip (a) the layout, and (b) a die micrograph.

Figure 74 shows the FFT results of the ADC measurement.

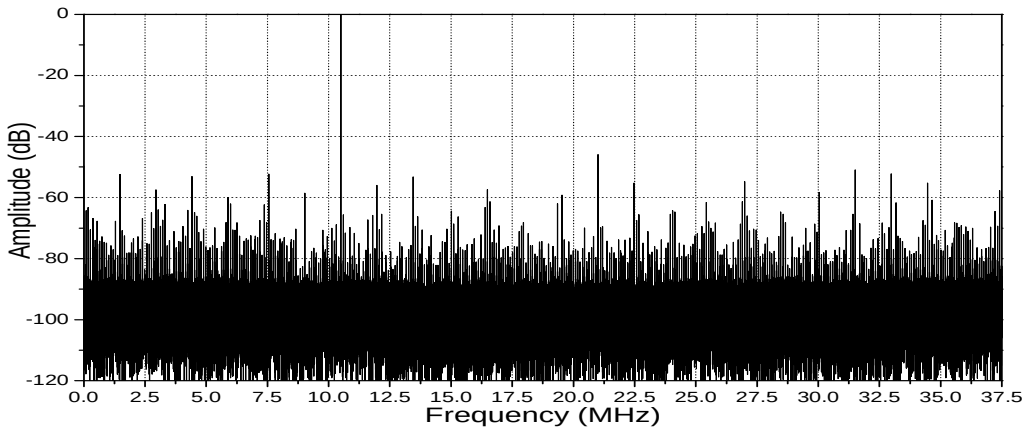


Figure 74: Measured output FFT spectrum of the ADC.

The signal generator clock was synchronized to the ADC clock. A test input frequency (f_{in}) of 10.50367355 MHz and a clock frequency (f_{clk}) of 75 MHz were chosen for coherent sampling as they prevent spectral leakage without window. With an input signal level of 3.6 $V_{pp-diff}$, the ENOB was 6.35 b from 262,144-point FFT. In the above operating conditions, power consumption of the ADC core was 78.38 mW.

Therefore, not only the ADC was operating successfully, but also f_{clk} was increased by 3.9 times from the previous ADC. Also, it can be seen that the gain mismatch component due to the interleaving of two ADCs was located at $f_{clk}/2 - f_{in} \approx 27$ MHz and not significant.

CHAPTER VI

CONCLUSION AND FUTURE WORK

6.1 Technical Contributions and Achievements

Over the past several years, we have observed rapid and widespread interest in MIMO technology in both mobile communication applications and radars. Although MIMO technology has great potential for greatly improving a current radar when combined with the CMOS technology, the exponentially increasing signal processing burden has not received as much attention so as it deserves.

This research proposes a new system architecture for a viable MIMO subsystem in the CMOS technology and also investigates its block level designs such as an ADC and a comparator. The research provides both theoretical contributions and successful implementations of the fully-integrated CMOS analog pulse compressor (APC) and an important sub-block with a low-power ADC. It also presents, as an important sub-block of a low-power ADC, an enhanced input range dynamic comparator. The achievements can be summarized as follows.

- To relax the requirements of speed and power for the ADC and the DSP, this research proposed a fully-integrated APC in a mixed-signal domain using an analog correlator and an AWG.

- The proposed fully-integrated APC was implemented with a CMOS 0.18-μm technology with core size of $3.13 \times 1.81\,\text{mm}^2$ and validated with results from various measurements using chirp signals and NLFMs.

- The detailed block specifications and structures of the AWG, the analog correlator, and the ADC were described, and the system evaluation using proposed

SNR and DR equations was performed. The results of the evaluation show that the proposed APC consumed about 62.6 mW when it was fully functional with a 1.8 V supply voltage, and the average SNR measured were 8.26 dB when a 1024-point chirp signal was used, and 18.09 dB when a 1024-point NLFM signal was used. The average DR measured were 12.08 dB when a 1024-point chirp signal was used, and 20.54 dB when a 1024-point NLFM signal was used.

- The SNR and the DR of the correlator were measured separately. The correlator alone had 32.69 dB of SNR and 28.20 dB of DR, respectively. The system timing was verified using multiple chirp signals.

- An enhanced input range dynamic comparator was proposed for the reduction of the size and power consumption of an ADC, and its input range was compared with that of a conventional dynamic comparator using calculations and simulations. The calculations and simulations showed that the CIDC had an enhanced input range while keeping the same trip point as a conventional comparator without additional stages or higher power consumption. Monte Carlo simulation results indicated that the CIDC was robust to device mismatches with only a minor speed penalty.

- Also proposed was a new ADC, which combines a pipeline architecture and an asynchronous sample-and-hold multiplying SAR as an important sub-block of the whole system. By exploiting metastability, the ASHMSAR achieved a smaller residue with less hardware than a conventional SAR.

- Detailed circuit implementations of the ASHMSAR including the op amp were described, and the timing related to metastability was mathematically analyzed. A calibration algorithm was also described, and circuit level simulation verified the performance of the design.

- A new ADC was implemented, and the performance was measured.

6.2 Future Research Directions

The implementation issues of a MIMO array for wireless communication applications or radars are not yet fully mature. Even though the theory itself is well established, a lot of important issues such as signal processing burdens still remain to be resolved for wider and far-reaching application of the theory.

To this end, two important contributing factors could be the CMOS technology and a new system architecture perspective. However, these factors can be addressed properly only with a good understanding of the multi-faceted problems encompassing the communication theory, system architectures, and circuit implementations. Therefore, collaboration among various disciplines may be required.

Meanwhile, from a sub-block level, an ADC is still a challenge for system evolution. Even though good progress in this area has been reported in recent years, mixed-signal integration still remains a great challenge for researchers in this area. Research of mixed-signal integrated circuits also requires wide background in areas such as signal processing on top of the circuit theory. Also, the fact that significant resources required to implement a large block such as an ADC hinders and limits access for researchers from academic areas. Collaboration among disciplines and industry could be very helpful to yield practical and innovative breakthroughs in this area. For a designer of mixed-signal integrated circuits, wide experience in various designs including both digital and analog, and experience in different architectures of ADC could be beneficial since one architecture alone may not be able to solve the challenges of the high-performance requirements which data converters face today.

RELATED PUBLICATIONS

[1] T. Song, S. M. Lee, J. Park, J. Hur, Michael Lee, K. Kim, C.-H. Lee, Franklin Bien, K. Lim, and J. Laskar, "Low-power technique for SRAM-based on-chip arbitrary waveform generator," *IEEE Trans. Instrum. Meas.*, accepted.

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[4] T. Song, J. Park, S. M. Lee, J. Choi, K. Kim, C.-H. Lee, K. Lim, and J. Laskar, "A 122-mW low-power multiresolution spectrum-sensing IC with self-deactivated partial swing techniques," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 3, pp. 188-192, Mar. 2010.

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[8] J. Park, T. Song, J. Hur, S. M. Lee, J. Choi, K. Kim, K. Lim, C.-H. Lee, H. Kim, and J. Laskar, "A fully integrated UHF-band CMOS receiver with multi-resolution spectrum sensing (MRSS) functionality for IEEE 802.22 cognitive radio applications," *IEEE J. of Solid-State Circuits*, vol. 44, no. 1, pp. 258-268, Jan. 2009.

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